A 1044500

APPLICATION	
NEXT ASSY	USED ON
1044476	477
	477A
	486
	633
	634
	662

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	ON SHEET 6 GROUND CONUCTOR WAS #4	6/29/82	K.M. Mauldin
B	ADDED SECTION NO 4.2.2.7. CHANG'D NOTE 3 (LOGO WAS DEPRESSED). CHANGD TOLERANCES ON DIM NO. 311 AND ADDAD NOTE FOR IDENTIFICATION MARK	11/2/82	K.M. Mauldin
	FORMAL RELEASE		
C	ECN 104910 C. SALAS 1/11/83 (1) EXTENSIVE REVISIONS	1/13/83	K.M. Mauldin
D	ECN 107114 D.HORTON 6/2/83 (1) EXTENSIVE REVISIONS	6/3/83	D. K.
E	ECN 108196 D.HORTON 9-19-83 (1) SH5, DELETED PARA. 6.1.3 (2) SH 7: #302 WAS ±.25; #307 WAS ±.18; #308 WAS ±.18; #332 WAS 3.28; #336 TOL. ADDED; #337 WAS #334.; #313 ADDED "MAX"	9/20/83	D. K
F	ECN 108330: R. Kalinowski 9/26/83 SH. 7: CHG'D. DIM TOL OF #321 WAS ⌖ A 0.12 & 329 WAS ⌖ B 0.12	9/26/83	D. K.
G	ECN 108987 DONALDSON 2-1-84 EXTENSIVE REVISIONS	3/5/84	BLL
H	ECN 108934 P. TAYLOR 4/2/84 chg. 6.1/ADD 6.2, 6.2.1, 6.2.2	4/4/84	BLL
J	ECN 108407 P. TAYLOR 4/2/84 AD 4.1.2 & 6/1.3--ADD TO SH 8	4/4/84	BLL
K	ECN 109532 P. TAYLOR 7/10/84 DLT.P.6.2.2; CHGED CHT.SH.7; ADD 662 APP.BLK.	7/13/84	Dpbi
M	[illegible]	ABD [illegible] ABD	

SHEET																										
REV STATUS	REV																									
OF SHEETS	SHEET	1	2	3	4	5	6	7	8																	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±1°
2 PLACE DECIMAL ± .010
3 PLACE DECIMAL ± .002

IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY

LOCATED OFF OOF:
DISK: 229
DOC: 4

		DATE
DWN	C. DARR	2/17/82
CHK	K.M. Mauldin	2/17/82
ENGR	K.M. Mauldin	2/17/82
QA	[illegible]	
APVD	[illegible]	2/17/82
CONTR NO		
DESIGN ACTIVITY RELEASE	[illegible]	2/17/82

TEXAS INSTRUMENTS
INCORPORATED
Lubbock, Texas

CABLE SPECIFICATION
8-CONDUCTOR PERIPHERAL

SIZE		DRAWING NO
A		1044500

SCALE [illegible] SHEET 1 OF 8

A 1052911

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	477	A	ECN 104911 BONNIE PARKER 9/29/83 SH.6- (1)DIM. IDENT. WERE ALPHABETICAL (2)DIM 606 WAS .015/.035, 611 WAS .115/.115, 612 WAS .115/.385, 613 WAS $15^{0}_{+1^{0}}$, AND DIM. 617 WAS .082/.050.	9/30/83	O.K.
	486				
	485				

	A	A	A	A																					
SHEET	24	25	26	27																					
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±1°
3 PLACE DECIMAL±.010
2 PLACE DECIMAL±.02

IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY

		DATE
DWN	C. SALAS	11/11/82
CHK	R. Kalinowski	1/12/83
ENGR	T. Skinner	1/15/83
QA		1/15/83
APVD		1/15/83
CONTR NO		
DESIGN ACTIVITY RELEASE	R. Kalinowski	2/1/83

TEXAS INSTRUMENTS
INCORPORATED
Lubbock, Texas

INTELLIGENT PERIPHERAL BIIS CONTROLLER SPECIFICATION

SIZE	DRAWING NO	
A	1052911	
SCALE		SHEET 1 OF 27

TI-81901A

OUTLINE

SIZE		DRAWING NO.
A		1052911
SCALE	REV A	SHEET 2

TI-22222

SIZE		DRAWING NO.
A		1052911
SCALE	REV A	SHEET 3

1.0 SCOPE:

THIS SPECIFICATION DETAILS THE REQUIREMENTS FOR AN INTELLIGENT PERIPHERALS BUS CONTROLLER (IBC). THIS IS A BUS CONTROLLER INTEGRATED CIRCUIT.

1.1 APPLICABLE DOCUMENTS:

THE FOLLOWING DOCUMENTS FORM A PART OF THIS SPECIFICATION TO THE EXTENT SPECIFIED HEREIN. UNLESS OTHERWISE INDICATED, THE REVISION AND ISSUE IN EFFECT ON THE DATE OF INVITATION FOR BIDS SHALL APPLY. IN THE EVENT OF ANY CONFLICT BETWEEN THIS DOCUMENT AND THE REFERRED DOCUMENTS, THIS DOCUMENT SHALL GOVERN.

1500005 - GENERAL REQUIREMENTS FOR IC'S
QRAs 10237 - PRODUCT QUALIFICATION
QRAs 10349 - IC QUALIFICATION

2.0 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE AIR TEMPERATURE RANGE:

SEE NOTE 1:

SUPPLY VOLTAGE, Vdd.....-0.5 TO +12 Vdc
INPUT/OUTPUT VOLTAGE, Vin.....-0.5 TO Vdd +5 Vdc
INPUT CURRENT, Iin.....+/- 10 mA
STORAGE TEMPERATURE, Tstg.....-40°C TO 125°C

NOTE 1: STRESSES BEYOND THOSE LISTED UNDER "ABSOLUTE MAXIMUM RATINGS" MAY CAUSE PERMANENT DAMAGE TO THE DEVICE. EXPOSURE TO ABSOLUTE MAXIMUM RATED CONSITIONS FOR EXTENDED PERIODS MAY AFFECT DEVICE RELIABILITY.

3.0 RECOMMENDED OPERATING CONDITIONS:

SUPPLY VOLTAGE, Vdd.....3 TO 7 Vdc
OPERATING TEMPERAUTRE, Top.....0°C TO 70°C.

4.0 D.C. CHARACTERISTICS:

Top = 0°C TO 70°C, Vdd = 5 Vdc, Vss = 0 Vdc, SEE NOTE 2.

	MIN	MAX	UNITS
INPUT LOW VOLTAGE (TTL INTERFACE), Vil1.....		0.8	V
INPUT LOW VOLTAGE (CMOS INTERFACE), Vil2.....		1.5	V
INPUT HIGH VOLTAGE (TTL INTERFACE), Vih1.....	2.0		V
INPUT HIGH VOLTAGE (CMOS INTERFACE), Vih2.....	3.5		V
OUTPUT LOW VOLTAGE (TTL INTERFACE), Iol = 1 mA, Vol1.....		0.4	V
OUTPUT LOW VOLTAGE (IRQ OUTPUT), Iol = 2 mA, Vol2.....		0.4	V
OUTPUT LOW VOLTAGE (CMOS INTERFACE), Iol = 4 mA, Vol3.....		0.4	V
OUTPUT HIGH VOLTAGE (TTL INTERFACE), Iol = -1 mA, Voh1.....	2.4		V
OUTPUT HIGH VOLTAGE (CMOS INTERFACE AND IRQ)		OPEN DRAIN	
INPUT LOW CURRENT (ALL INPUTS), Iil.....-1		.1	uA
INPUT HIGH CURRENT (ALL INPUTS), Iih.....-1		1	uA
OUTPUT 3 STATE CURRENT (TTL INTERFACE), Ioz....-10		10	uA
STANDBY CURRENT, Idd.....		250	uA
INPUT CAPACITANCE, Cin.....		10	pF

NOTE 2: TTL INTERFACE - I/O0-I/O3, CS, RS, E, R/W, O0-O2, MS
CMOS INTERFACE - D0-D3, HSK, BAV, RES

5.0 REQUIREMENTS:

5.1 PHYSICAL:

22 - PIN, DUAL-IN-LINE PACKAGE. SEE FIGURE 1.

5.1.1 LEADS:

SOLDERABLE PER MIL-STD-883, METHOD 2003, WITHOUT AGING.

5.1.2 PIN CONFIGURATION:

SEE FIGURE 2.

5.1.3 MARKING:

PARTS SHALL BE MARKED WITH THE MANUFACTURER'S IDENTIFICATION, TI PART NUMBER AND DATE CODE.

3.2 SIGNAL RISE/FALL TIMES:

THE CHART BELOW GIVES THE SPECIFIED AC CHARACTERISTICS OF ALL BUS LINES. THE RISE AND FALL TIMES FOR THIS CHART ARE BETWEEN 10% AND 90% OF VDD. THE OPERATING TEMPERATURE RANGES FROM 0 C TO 70 C.

HEX BUS AC SPECIFICATION

PARAMETER	MAX.	UNITS
RISE TIME	3.5*	uSEC.
FALL TIME	2.5*	uSEC.

* THESE TIMES ARE CALCULATED FROM INITIATION OF THE SIGNAL TRANSITION (INCLUDING PROPAGATION TIME THROUGH ANY BUS INTERFACE DEVICES) AND ARE TERMINATED WHEN THE LEVEL REACHES 0.4V FOR FALL TIMES AND 4.0V FOR RISE TIMES.

3.3 NOMINAL DEVICE VALUES:

THE EQUIVALENT CAPACITANCE OF A TYPICAL DEVICE IS 200 pF (NOT INCLUDING THE CEQ OF THE CABLE AND CONNECTOR) AND SHOULD BE CONNECTED TO THE BUS WITH A 8.2K OHM PULL-UP RESISTOR. A DEVICE WITH A HIGHER CEQ SHOULD BE CONSIDERED AS TWO (OR MORE) DEVICES AND THE RPULL-UP OF THIS DEVICE SHOULD BE DECREASED ACCORDINGLY. THIS WILL AFFECT THE NUMBER OF PERIPHERALS ALLOWED ON THE BUS. NOTE THAT WHEN CALCULATING THE VALUE OF THE PULL-UP RESISTANCE USED, THE 30pF EQUIVALENT CAPACITANCE OF THE CABLE AND CONNECTOR MUST BE CONSIDERED.

1. PULL-UP RESISTORS ARE 8.2 KOHMS +/- 10%.
2. Cin FOR EACH DEVICE IS 20 pF.
3. Ccable = 20pF / FT.
4. Cconnector = 10 pF.
5. 180 pF CAPACITORS ARE USED ON ALL OUTPUTS TO MINIMZE RFI AND CROSSTALK PROBLEMS.

1. SCOPE:

THIS SPECIFICATION COVERS THE FUNCTIONAL CAPABILITIES AND THE MECHANICAL AND ELECTRICAL REQUIREMENTS FOR EIGHT CONDUCTOR PERIPHERAL CABLE ASSEMBLY.

2. APPLICABLE DOCUMENTS:

THE FOLLOWING DOCUMENTS FORM A PART OF THIS SPECIFICATION TO THE EXTENT SPECIFIED HEREIN. UNLESS OTHERWISE INDICATED, THE REVISION AND ISSUE IN EFFECT ON THE DATE OF INVITATION FOR BIDS SHALL APPLY. IN THE EVENT OF ANY CONFLICT BETWEEN THIS DOCUMENT AND THE REFERRED DOCUMENTS, THIS DOCUMENT SHALL GOVERN.

SPECIFICATIONS FOR PCB MOUNT DOUBLE ROW RIGHT ANGLE HEADER TI PART NUMBER 1044501.

3. GENERAL DESCRIPTION:

THE PERIPHERAL CABLE SHALL SERVE AS THE COMMUNICATION LINK BETWEEN A VARIETY OF CALCULATORS AND PERIPHERALS OR PERIPHERAL ADAPTERS. IT WILL BE AN EIGHT CONDUCTOR CABLE, PROVIDED WITH IDENTICAL PLUGS AT IT'S BOTH ENDS.

4. REQUIREMENTS

4.1 MATERIALS:

EXCEPT AS OTHERWISE SPECIFIED, THE SELECTION OF MATERIALS SHALL BE AT THE DISCRETION OF THE CONTRACTOR. MATERIALS SHALL BE SUCH THAT THE PERFORMANCE AND PRODUCT CHARACTERISTICS SPECIFIED HEREIN WILL BE MET WHEN EXPOSED TO THE SPECIFIED STORAGE OR ENVIRONMENTAL CONDITIONS.

4.1.2 THE PLUG AND CABLE COLOR SHALL MATCH BORG WARNER LIGHT GREY COLOR NO. 33143.

SIZE A

SIZE A

SHEET 2

4.2 MECHANICAL SPECIFICATIONS AND CONSTRUCTIONS

4.2.1 THE CABLE ASSEMBLY SHALL MEET THE REQUIREMENTS SPECIFIED IN FIG. 1 AND FIG. 2. ALL PLUGS SHALL INCLUDE APPROPRIATE STRAIN RELIEF CAPABLE OF SUSTAINING ALL SPECIFIED MECHANICAL TESTS.

4.2.2 CONNECTORS

4.2.2.1 THE EIGHT POSITION PLUG SHALL BE MOLDED FROM THERMOPLASTIC WITH APPROPRIATE STRAIN RELIEF AND SHALL CONFORM TO THE SHAPE AND SIZE SPECIFIED IN FIG. 2. THE PLUG BODY SHALL BE MOLDED AROUND THE CONNECTOR HOUSING SUCH THAT THERE IS NO AIR PATH TO THE CONNECTORS FROM THE OUTSIDE EXCEPT FROM THE FRONT SURFACE.

4.2.2.2 THE PLUG SHALL MATE WITH DOUBLE ROW PCB MOUNT RIGHT ANGLE HEADER, TI PART NO. 1044501.

4.2.2.3 THE PLUG SHALL BE CONNECTED TO THE TWO ENDS OF THE CABLE SUCH THAT WHEN THE CABLE IS LYING STRAIGHT ON A FLAT SURFACE, THE OPPOSITE FACES OF THE TWO PLUGS WILL FACE UP.

4.2.2.4 THE CONNECTOR IN THE PLUG SHALL BE RESTRAINED FROM MOVING DURING WITHDRAWAL AND INSERTION OF THE PLUG. THE CONNECTORS SHALL BE POSITIONED IN THE PLUG, SUCH THAT 5.84 ± .50 LONG PIN SHALL YIELD FULL CONTACT.

4.2.2.5 A METAL RING SOLDERED TO THE GROUND CONDUCTOR SHALL BE PROVIDED AROUND THE CONNECTOR HOUSING AS SHOWN IN FIG. 2 THE MATAL RING MATERIAL SHALL BE .254 MM THICK, (301) HALF HARD CARTRIDGE BRASS ALLOY 230. THE METAL RING SHALL BE TIN LEAD PLATED AND POSITIONED AROUND THE CONNECTOR HOUSING SUCH THAT IT IS FLUSH TO THE FRONT SURFACE PF THE PLUG WITHIN .12MM. (302)

4.2.2.6 "THE PLUG SURFACES SHALL BE FREE FROM ALL BUT .10 mm OF FLASH, SINK MARKS, SCRATCHES AND ANY OTHER MOLDING DEFECTS."

4.2.2.7 THE FRONT EDGE OF THE CONNECTORS INSIDE THE PLUG SHALL BE MINIMUM .38 MM AWAY FROM THE FRONT SURFACE OF THE PLUG. (303)

4.2.3 CABLE CONDUCTORS

4.2.3.1 THE CABLE CROSS-SECTIONAL DIMENSIONS SHALL CONFORM TO FIGURE 1. THE CABLE INSULATION SHALL BE ON PVC.

DIMENSION IDENTIFICATION	
USED	NOT USED
301-303	

SIZE A | DRAWING NO. 1044500 | SCALE | REV K | SHEET 3

4.2.3.2 THE CABLE SHALL CONSIST OF 8 CONDUCTORS AND EACH SHALL BE OF 26/28 AWG STRANDED CONSTRUCTION. EACH CONDUCTOR SHALL HAVE 300 VOLTS DC INSULATION.

4.2.4 MECHANICAL STRENGTH TESTING

4.2.4.1 THE CABLE SHALL BE CAPABLE OF SUSTAINING 400 CYCLES OF FLEX TESTING IN WHICH A ½ LB. WEIGHT IS HUNG ON THE CABLE AND THE PLUG IS ROTATED ABOUT ITS MINOR AXIS AT THE POINT OF CABLE AND PLUG CONNECTION THRU A 180^0 ARC.

4.2.4.2 THE CABLE SHALL BE CAPLABLE OF SUSTAINING A PULL LOAD OF 20 LBS FOR ONE MINUTE. THE PULL LOAD SHALL BE APPLIED BY MOUNTING THE PLUG RIGIDLY AND TENDING TO PULL THE CABLE OUT OF THE PLUG.

4.2.4.3 BOTH TESTS MENTIONED IN 4.2.4.1 AND 4.2.4.2 SHALL APPLY TO BOTH PLUGS. THE CABLE SHALL CONTINUE TO MEET ALL ELECTRICAL REQUIREMENTS OF SECTION 4.3 AFTER EACH TEST AND SHOULD NOT DEVELOP ANY DISCONTINUITY OR SHORTING OF CONDUCTORS.

4.2.4.4 THE PLUG SHALL BE CAPABLE OF SUSTAINING 5000 CYCLES OF INSERTION-WITHDRAWAL WITH TI PART NO. 1044501-1, SUCH THAT AFTER THIS TEST THE PULL OUT AND INSERTION FORCE SHALL NO FALL BELOW 1.0LB OR EXCEED 5.0LBS. ALSO THE TOTAL RESISTANCE OF ANY ONE OF THE CONDUCTORS, INCLUDING THE CONTACT RESISTANCE BETWEEN THE CONNECTOR AND THE PIN AT ITS TWO ENDS, SHALL NO EXCEED .4 OHMS.

4.3 <u>ELECTRICAL SPECIFICATIONS:</u>

4.3.1 CURRENT RATING: 100 MA NOMINAL FOR SIX CONDUCTORS, AND 500 MA NOMINAL FOR CONDUCTORS 1 & 6 (VIEW B-B).

4.3.2 VOLTAGE RATINGS: 15 VOLTS MAXIMUM.

4.3.3. THE CAPACITANCE SHALL NOT EXCEED 100 PICOFARADS FOR 914 MM ASSEMBLY & 60 PF FOR 152 MM ASSEMBLY.

4.3.4 THE TOTAL SERIES RESISTANCE SHALL BE A MAXIMUM OF .4 OHMS FOR ANY CONDUCTOR, INCLUDING THE CONTACT RESISTANCE BETWEEN THE CONNECTOR AND THE PIN.

4.3.5 MINIMUM ISULATION RESISTANCE BETWEEN ANY TWO CONDUCTORS SHALL EXCEED 10 M OHMS WITH 15 VOLTS APPLIED.

SIZE		DRAWING NO.	
A		A	1044500
SCALE	REV K		SHEET 4

4.4. ENVIRONMENTAL REQUIREMENTS:

4.4.1 OPERATING ENVIRONMENT: 0^0C TO $+70^0$, 85% RELATIVE HUMIDITY.

4.4.2 STORAE TESTS: -40^0C FOR 1000 HOURS, $+70^0$C FOR 1000 HOURS, 50^0C AT 95% RH FOR 360 HOURS.

4.4.3 THE CABLE SHALL OPERATE STISFACTORILY AND CONTINUE TO MEET ALL MECHANICAL AND ELECTICAL SPECIFICATIONS AFTER THE STORAGE TESTS.

4.5 PRODUCT ASSURANCE:

THE MANUFACTURER SHALL PERFORM SUFFICIENT TESTS TO INSURE THAT ALL DEVICES SUPPLIED TO THIS SPECIFICATION SHALL MEET THE REQUIREMENTS OF THIS SPECIFICATION.

5.0 QUALITY ASSURANCE PROVISIONS:

5.1 UNLESS OTHERWISE SPECIFIED IN THE CONTRACT OR PURCHASE ORDER THE SUPPLIER IS RESPONSIBLE FOR THE PERFORMANCE OF ALL INSPECTION REQUIREMENTS AS SPECIFIED HEREIN. EXCEPT AS OTHERWISE SPECIFIED IN THE CONTRACT OR ORDER, THE SUPPLIER MAY USE HIS OWN OR ANY OTHER FACILITIES SUITABLE FOR THE PERFORMANCE OF THE INSPECTION REQUIREMENTS SPECIFIED HEREIN, UNLESS DISAPPROVED BY THE PROCURING ACTIVITY.

5.1 CONTINUED

THE PROCURING ACTIVIT RESERVES THE REGHT TO PERFORM ANY OF THE INSPECTIONS SET FOR TH IN THE SPECIFICATION WHERE SUCH INSPECTIONS ARE DEEMED NECESSARY TO ASSURE SUPPLIES AND SERVICES CONFORM TO PRESCRIBED REQUIREMENTS.

6.0 PREPARATION FOR DELIVERIES

6.1 EACH PACKING CONTAINER SHALL BE LEGIBLY MARKED WITH THE MANUFACTURER'S PART NUMBER, THE DATE OF SHIPMENT, AND QUANTITY.

6.1.3 IN SHIPPING PACKAGE, THE CABLES SHALL BE SUPPLIED IN BUNDLES OF 50 AND EACH BUNDLE SHALL BE LEGIBLY MARKED WITH DATE OF SHIPMENT AND MANUFACTURER'S INDENTIFICATION MARK.

SIZE	DRAWING NO.
A	1044500
SCALE	REV K
	SHEET 5

TI-82222

6.2 PACKAGING

6.2.1 BULK

PACKAGING SHALL BE ADEQUATE TO PROVIDE PROTECTION AGAINST DAMAGE, BREAKAGE, OR LOSS DURING SHIPMENT FROM THE SUPPLY SOURCE TO THE ULTIMATE USING ACTIVITY. PACKAGES SHALL BE OF A TYPE NOT DESTROYED BY OPENING.

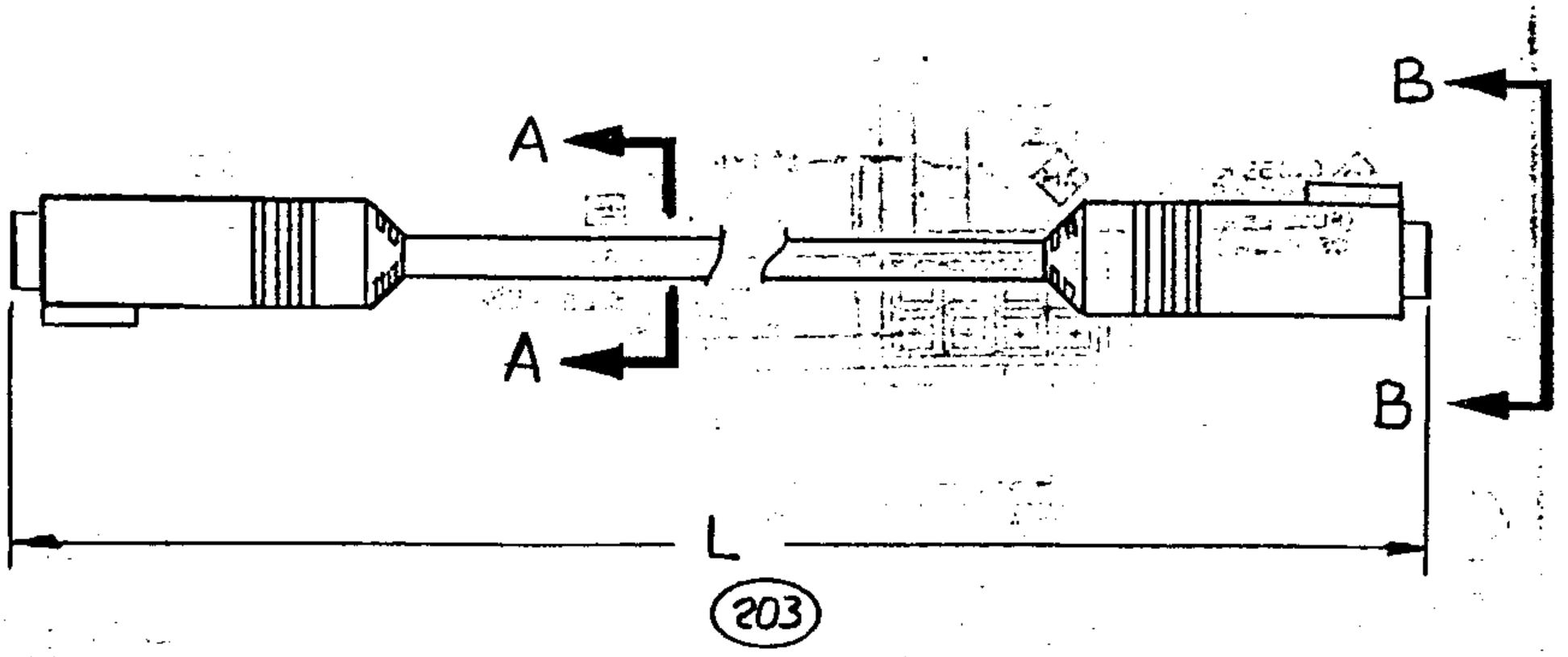
NOTES UNLESS OTHERWISE SPECIFIED:

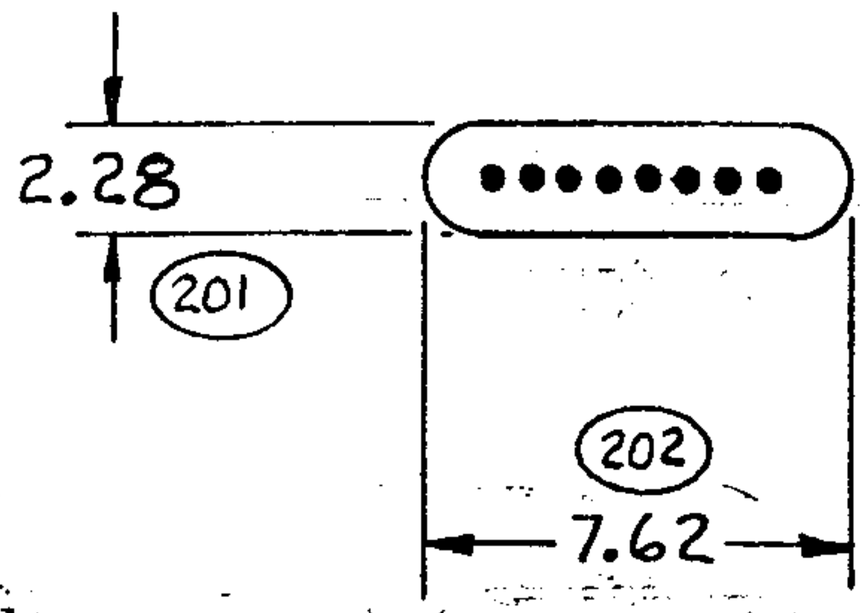
6. TOLERANCES:
   ANGLES: ± 1^0
   1 PLACE DECIMAL: ± .5
   TWO PLACE DECIMALS: ± .12
   THREE PLACE DECIMALS: ± .08
5. NUMBERS LOCATED IN ◇ AND ⬭ ARE FOR DEMENSIONS IDENTIFICATION ONLY. (SEE CHART EACH SHEET).
4. TOLERANCES ARE NON-CUMULATIVE.
3. TI LOGO TO BE RAISED 0.3MM. (601)
2. BREAK ALL SHARP EDGES.
1. ALL DIMENSIONS ARE IN MILLIMETERS.

DIMENSION IDENTIFICATION	
USED	NOT USED
601	

SIZE		DRAWING NO.	
A		A	1044500
SCALE 1	REV K		SHEET 6

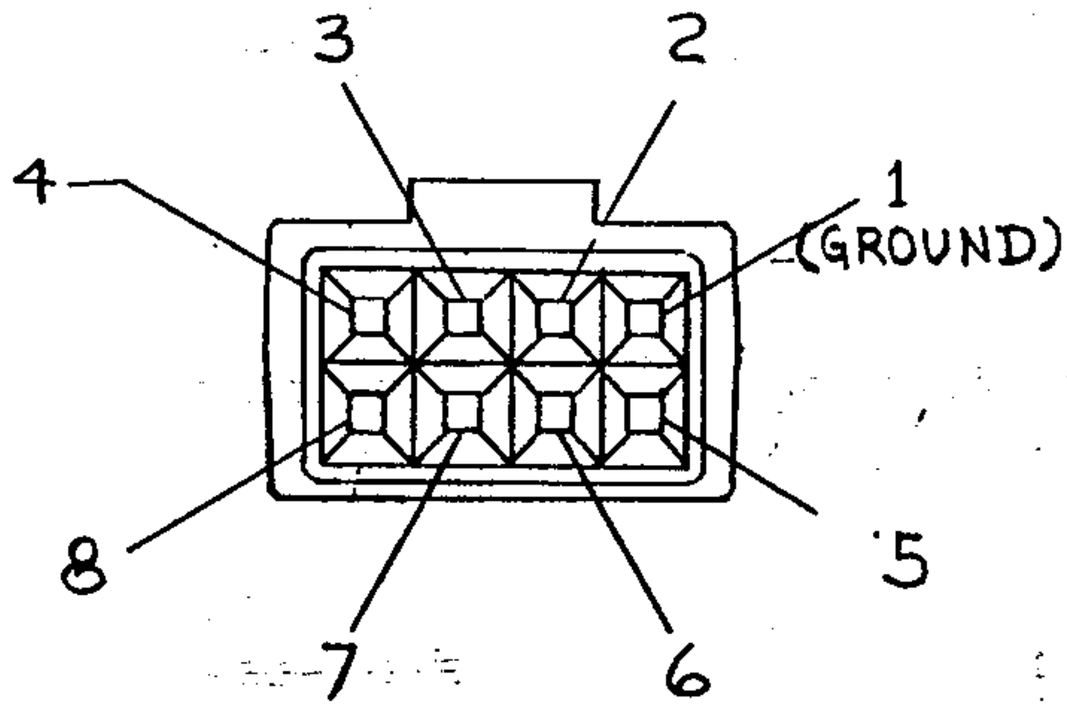
TI-22222





SECTION A-A

SCALE: 4/1



VIEW B-B

SCALE: 10/1

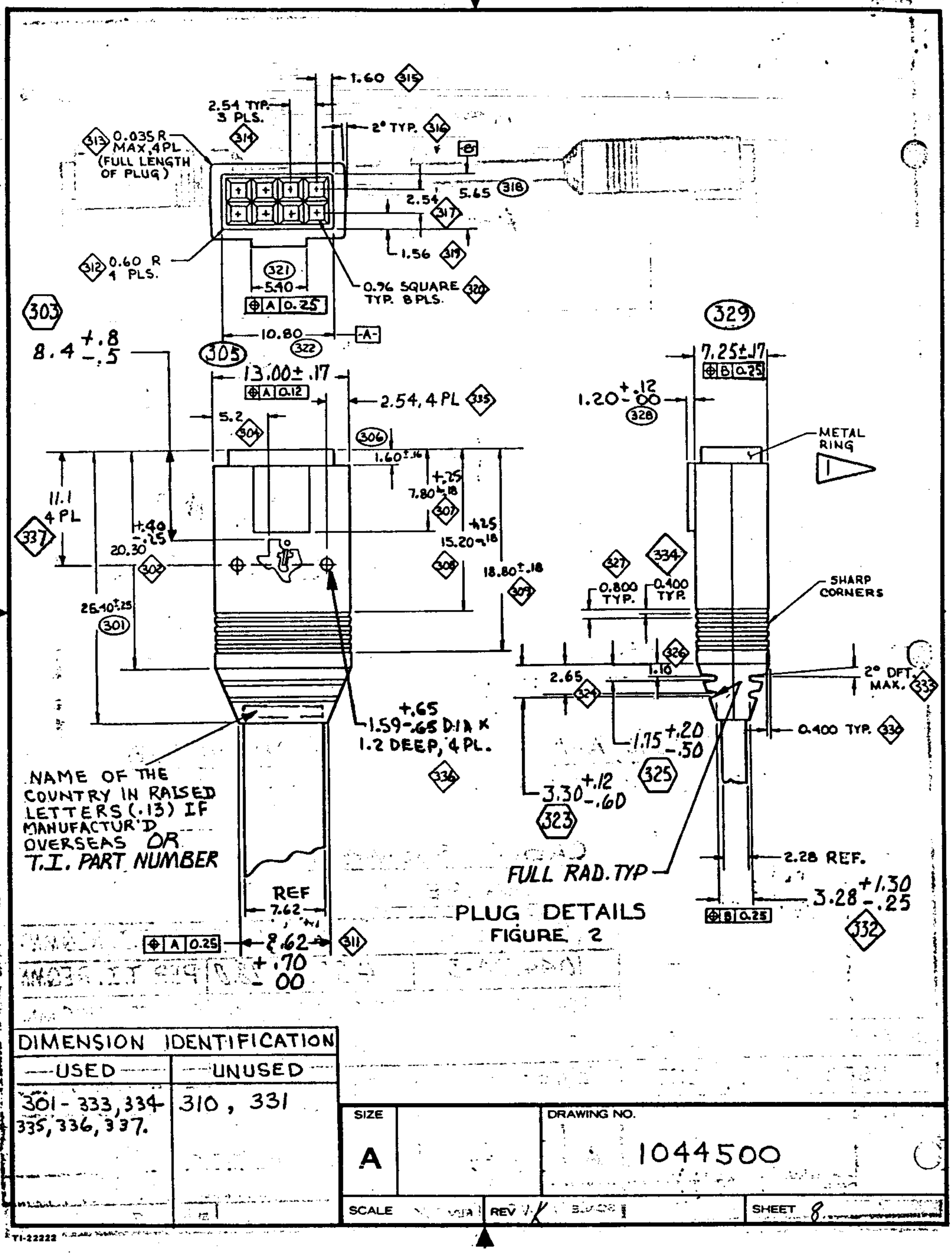
CABLE ASSEMBLY

FIGURE 1

PART NO.	DIM. "L"	COLOR
1044500-4	1219.0 ± 25.0	PER T.I. REQMNT
1044500-3	457.0 ± 18.0	PER T.I. REQMNT
1044500-2	203.0 ± 12.0	PER TI REQMNT
1044500-1	914.0 ± 25.0	PER TI REQMNT

DIMENSION IDENTIFICATION	
USED	UNUSED
201 — 203	

SIZE A | DRAWING NO. 1044500 | SCALE NONE | REV K | SHEET 7



PLUG DETAILS
FIGURE 2

DIMENSION IDENTIFICATION	
USED	UNUSED
301 - 333, 334 335, 336, 337.	310, 331

SIZE A		DRAWING NO. 1044500	
SCALE	REV K		SHEET 8

TI-22222

A 1056477

APPLICATION	
NEXT ASSY	USED ON
	631
	477
	485
	486
	601
	608
	612
	617
	630
	633
	634
	635
	636
	638

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±1°
3 PLACE DECIMAL ±.010
2 PLACE DECIMAL ±.02

IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY

LOCATION: OOF
DISK: 129
DOC: 1-2

DRN D. HORTON 6/20/83 DATE
CHK [illegible signature] 7/2/83
ENGR [illegible signature]
QA [illegible signature]
APVD [illegible signature]
CONTR NO
DESIGN ACTIVITY RELEASE [illegible signature] 9/12/83

TEXAS INSTRUMENTS
INCORPORATED
Lubbock, Texas

SPECIFICATIONS: HEX BUS ELECTRICAL

SIZE A

DRAWING NO 1056477

SCALE

SHEET 1 OF 14

TI-3100A

SECTION 1

OVERVIEW

1.1 PURPOSE OF THIS DOCUMENT:

THIS DOCUMENT IS A COMPLETE ELECTRICAL SPECIFICATION FOR THE HEX BUS (Tm) CMOS BUS USED TO CONNECT INTELLIGENT PERIPHERALS TO CALCULATOR OR SMALL COMPUTER TYPE PRODUCTS. THIS DOCUMENT IS MEANT TO BE USED IN FORMULATING THE DETAILED ELECTRICAL DESIGN.

1.2 SCOPE OF THIS DOCUMENT:

THIS DOCUMENT DESCRIBES THE ELECTRICAL CHARACTERISTICS OF THE HEX BUS. BECAUSE THE PRIMARY PURPOSE IS ASSISTING IN ELECTRICAL DESIGN, SOFTWARE IS NOT DISCUSSED IN THIS DOCUMENT. FOR USER AND SOFTWARE ASSISTANCE, SEE "THE INTELLIGENT PERIPHERAL BUS: STRUCTURE, TIMING, AND PROTOCOL SPECIFICATION".

1.3 ORGANIZATION OF THIS DOCUMENT:

THE ELECTRICAL SPECIFICATIONS OF THE HEX BUS ARE DESCRIBED INDIVIDUALLY IN THE SECTIONS LISTED BELOW.

SECTION 1 - SIGNALS DESCRIPTION
SECTION 2 - TIMING CHARACTERISTICS
SECTION 3 - ELECTRICAL CHARACTERISTICS

1.4 TERMINOLOGY:

HSK - HANDSHAKE I/O CONTROL LINE
BAV - BUS AVAILABLE I/O CONTROL LINE
D0-D3 - FOUR DATA LINES ON THE HEX BUS

HEXBUS ADAPTOR

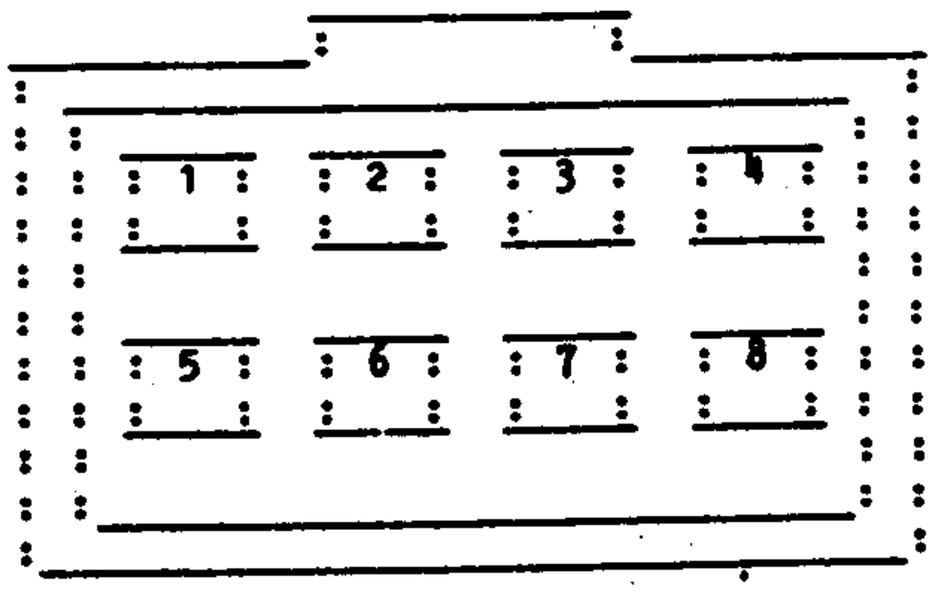
SECTION 2

SIGNALS DESCRIPTION

2.1 GENERAL INFORMATION:

THE HEX BUS CONTAINS EIGHT LINES, OF WHICH SEVEN ARE CURRENTLY IN USE. THE FUNCTION OF EACH OF THESE SEVEN ARE DISCUSSED IN THIS SECTION. THE EIGHT LINES ARE LISTED BELOW WITH A BRIEF DESCRIPTION OF EACH. THE DIAGRAM AT THE BOTTOM OF THE PAGE INDICATES THE RELATIVE LOCATION OF EACH LINE IN THE HEX BUS CABLE. FOR MORE INFORMATION REFER TO THE CABLE SPECIFICATION - TI#1044500.

D0-D1 - TWO LSB I/O DATA BITS ---------- PIN 1,2
BAV - BUS AVAILABLE, I/O TRAFFIC CONTROL LINE -PIN 3
GND - COMMON GROUND LINE ---------- PIN 4
HSK - HANDSHAKE, I/O TIMING CONTROL LINE ----- PIN 5
FUT - RESERVED FOR FUTURE USE ---------- PIN 6
D2-D3 - TWO MSB I/O DATA BITS ---------- PIN 7,8



RELATIVE PIN LOCATION WHEN LOOKING INTO THE CONNECTOR OF A HEX BUS CABLE.

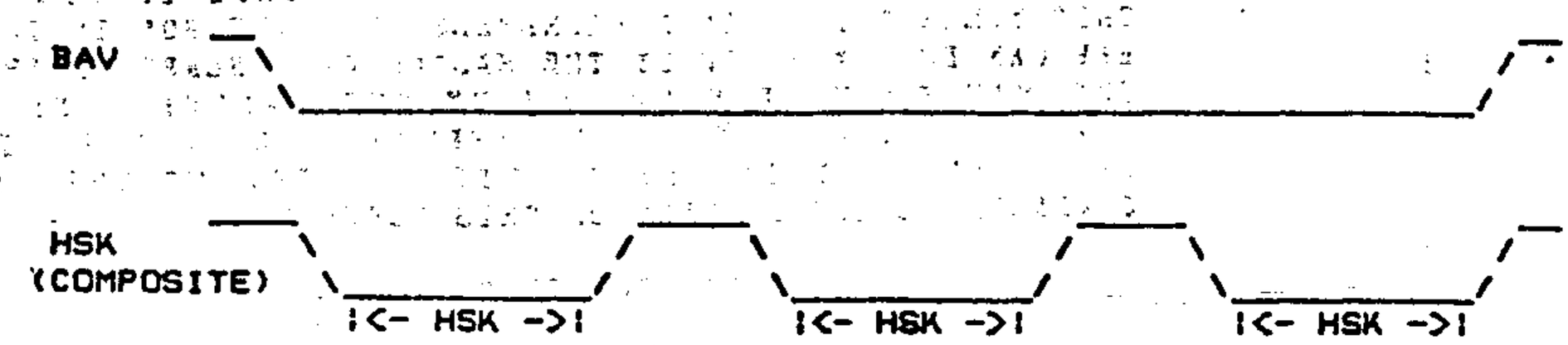
2.2 HSK - HANDSHAKE, I/O TIMING CONTROL LINE:

THE HSK LINE IS USED BY BOTH THE MASTER AND THE PERIPHERALS TO SIGNAL THE FACT THAT DATA IS ON THE LINE. HSK IS AN OPEN-DRAIN, CMOS OUTPUT IN ORDER TO ALLOW IT TO BE PULLED LOW BY ANY DEVICE ON THE BUS. A DEVICE WILL PULL HSK LOW TO SIGNAL TO THE OTHER DEVICES ON THE BUS THAT DATA IS AVAILABLE FROM THAT DEVICE WHICH MAY BE READ BY THE OTHER DEVICES ON THE BUS. IN ORDER TO PREVENT CROSS-TALK BETWEEN HSK AND THE DATA LINES (WHICH MAY CAUSE UNWANTED SPIKES ON THE HSK LINE), THE DATA SHOULD BE GATED OUT TO THE BUS BY THE LOW LEVEL OF THE HSK.

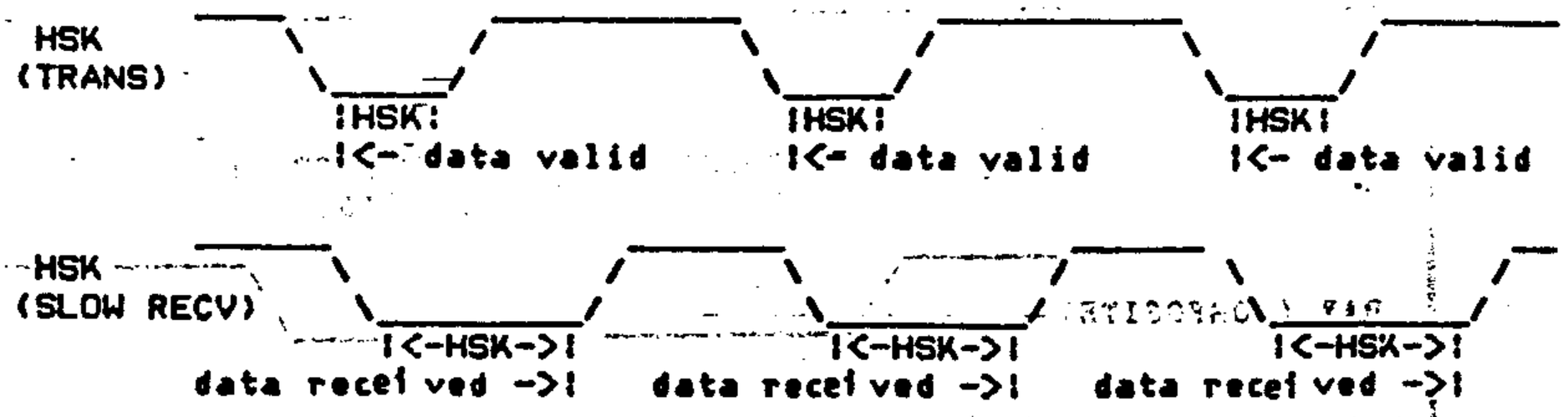
HSK WILL BE HELD LOW BY THE RECEIVING DEVICES UNTIL THEY HAVE LATCHED THE FOUR BITS OF DATA ON THE BUS. IF THE TRANSMITTER IS SLOWER THAN THE RECEIVERS, THE TRANSMITTER COULD BE THE DEVICE WHICH DETERMINES WHEN THE HSK LINE WILL GO HIGH. REFER TO THE DIAGRAM ON THE FOLLOWING PAGE FOR A BETTER UNDERSTANDING OF THIS COMMUNICATION PROCEDURE.

FOR MORE INFORMATION ON THE TIMING INVOLVED IN THIS TRANSACTION, REFER TO THE TIMING CHARACTERISTICS SECTION OF THIS DOCUMENT.

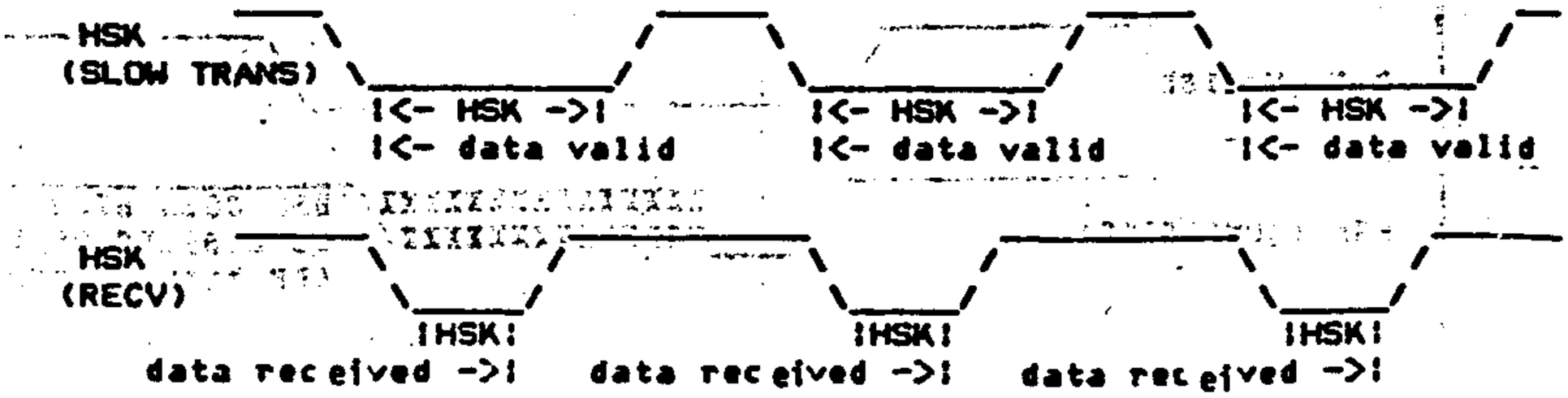
Hex Bus Handshake Sequence



HSK COMPONENTS - SLOW RECEIVER



HSK COMPONENTS - SLOW TRANSMITTER



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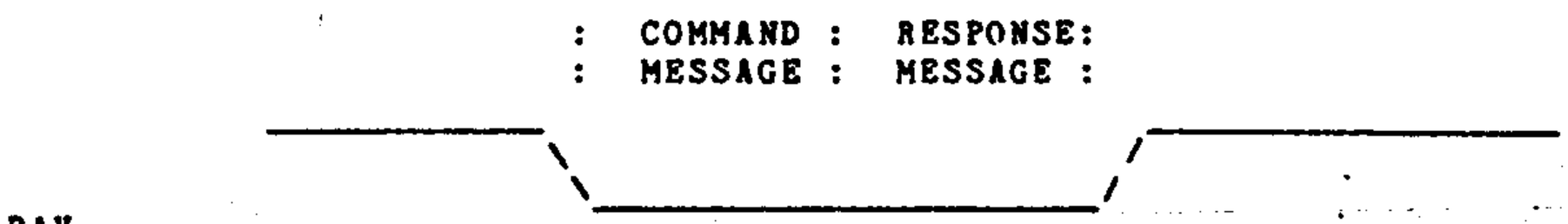
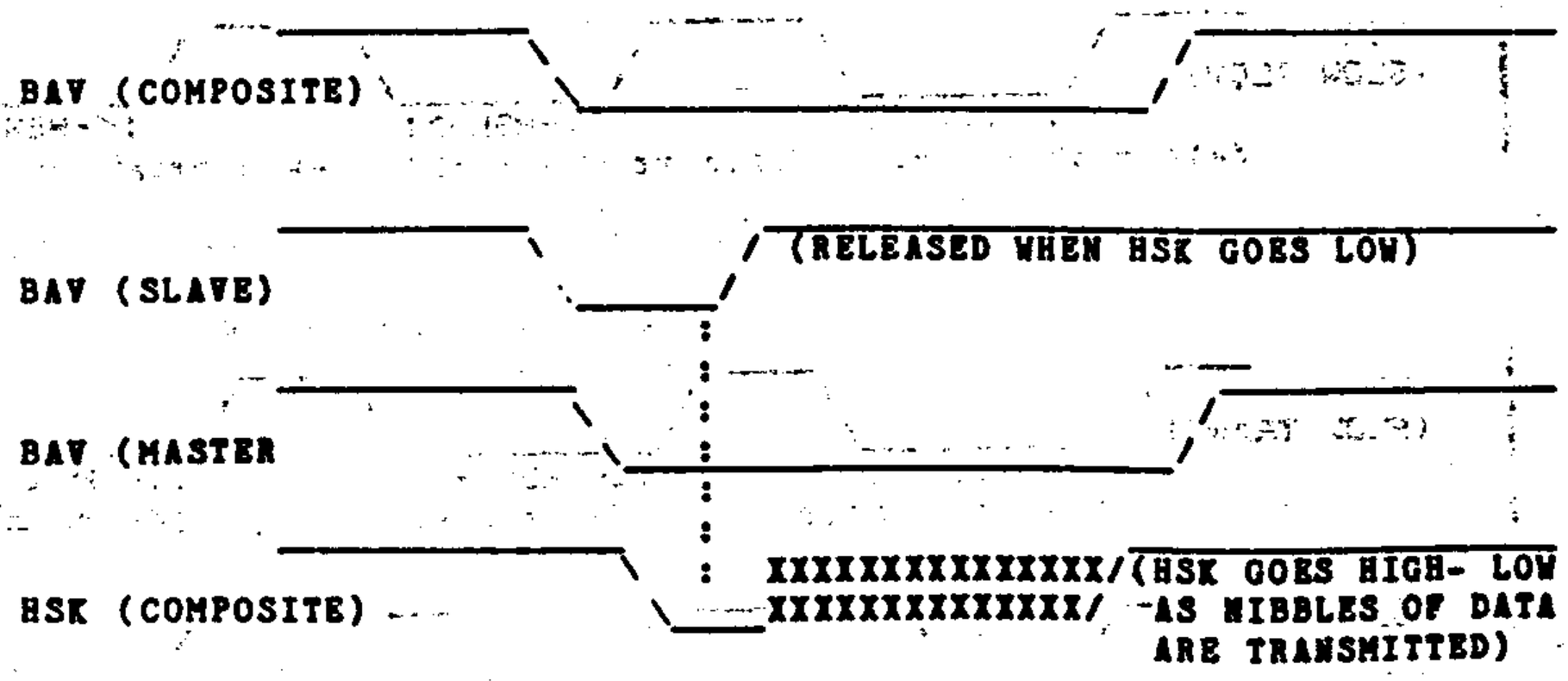
2.3 BAV - BUS AVAILABLE; I/O TRAFFIC CONTROL LINE:

EACH MESSAGE ON THE HEX BUS CONSISTS OF TWO PARTS, THE COMMAND MESSAGE AND THE RESPONSE MESSAGE. WHENEVER A MESSAGE TRANSFER IS IN PROGRESS, BAV WILL BE HELD LOW BY THE MASTER PERIPHERAL UNTIL THE MESSAGE IS COMPLETE. THIS TELLS THE OTHER PERIPHERALS THAT THE BUS IS IN USE. BAV CAN BE TAKEN LOW BY THE MASTER OR A SLAVE PERIPHERAL BUT MAY ONLY BE HELD LOW BY THE MASTER. SEE THE DIAGRAMS BELOW. FOR MORE INFORMATION ON THE TIMING INVOLVED IN THIS TRANSACTION, REFER TO THE TIMING CHARACTERISTICS SECTION OF THIS DOCUMENT.

BAV POLLED BY MASTER



BAV POLLED BY SLAVE - HELD BY MASTER



2.4 **D0-D3 - FOUR I/O DATA BITS:**

THESE FOUR BITS ARE USED TO SEND DATA ON THE HEX BUS ONE NIBBLE AT A TIME. THE LOWER NIBBLE OF THE 8 BIT BYTE WILL BE SENT FIRST, FOLLOWED BY THE MOST SIGNIFICANT NIBBLE. THE DATA LINES ARE CONFIGURED AS SHOWN BELOW:

DATA LINE CONFIGURATION

D3 - MOST SIGNIFICANT BIT
D2 - DATA BIT
D1 - DATA BIT
D0 - LEAST SIGNIFICANT BIT

2.5 **GND - FLOATING REFERENCE GROUND LINE:**

A COMMON GROUND LINE IS RUN TO ALL THE PERIPHERALS IN ORDER TO REFERENCE ALL VOLTAGES EQUALLY TO THE SAME POINT. THIS IS A SIGNAL REFERENCE AND SHOULD NOT BE USED AS A POWER LINE OR TIED TO EARTH-GROUND.

2.6 **FUT - RESERVED FOR FUTURE USE:**

SECTION 3

TIMING CHARACTERISTICS

3.1 GENERAL INFORMATION:

THIS SECTION WILL DEAL WITH THE TIMING OF THE VARIOUS SIGNALS OF THE HEX BUS. THE FIRST PART WILL DEAL WITH THE TIMING REQUIREMENTS OF THE SIGNALS LISTED IN SECTIONS 1 AND 2. THE SECOND PART WILL DEAL WITH ACTUAL RISE AND FALL TIMING PARAMETERS OF THE SIGNALS.

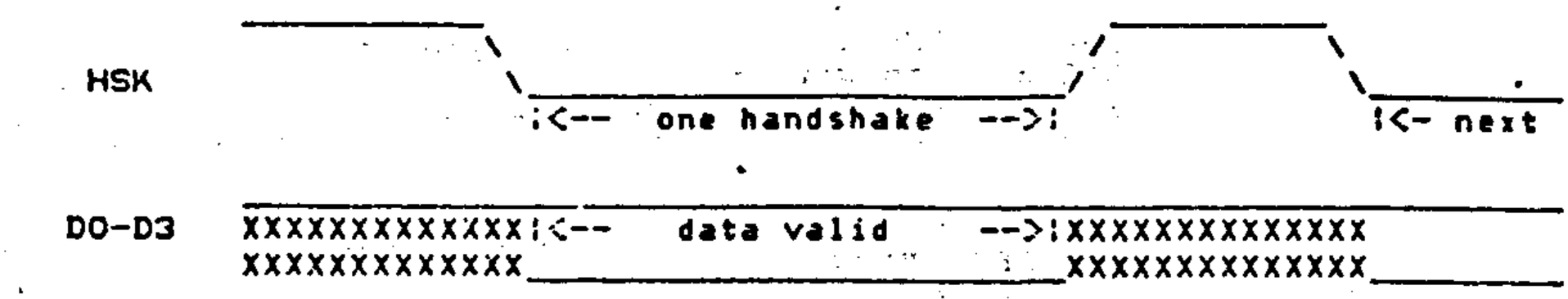
HANDSHAKE TIMING PARAMETERS

ITEM	MIN.(uSEC.)	MAX.(uSEC)
HSK LOW TO DATA VALID	-	0.5
HSK LOW(XMIT) TO HSK LOW(BUS)	-	3
HSK LOW(BUS) TO HSK LOW(RCV)	-	5
HSK LOW(XMIT) TO HSK HIGH(XMIT)	8	-
HSK HIGH TO DATA HIGH	0	2.5*
HSK HIGH TO HSK LOW	8	20,000**

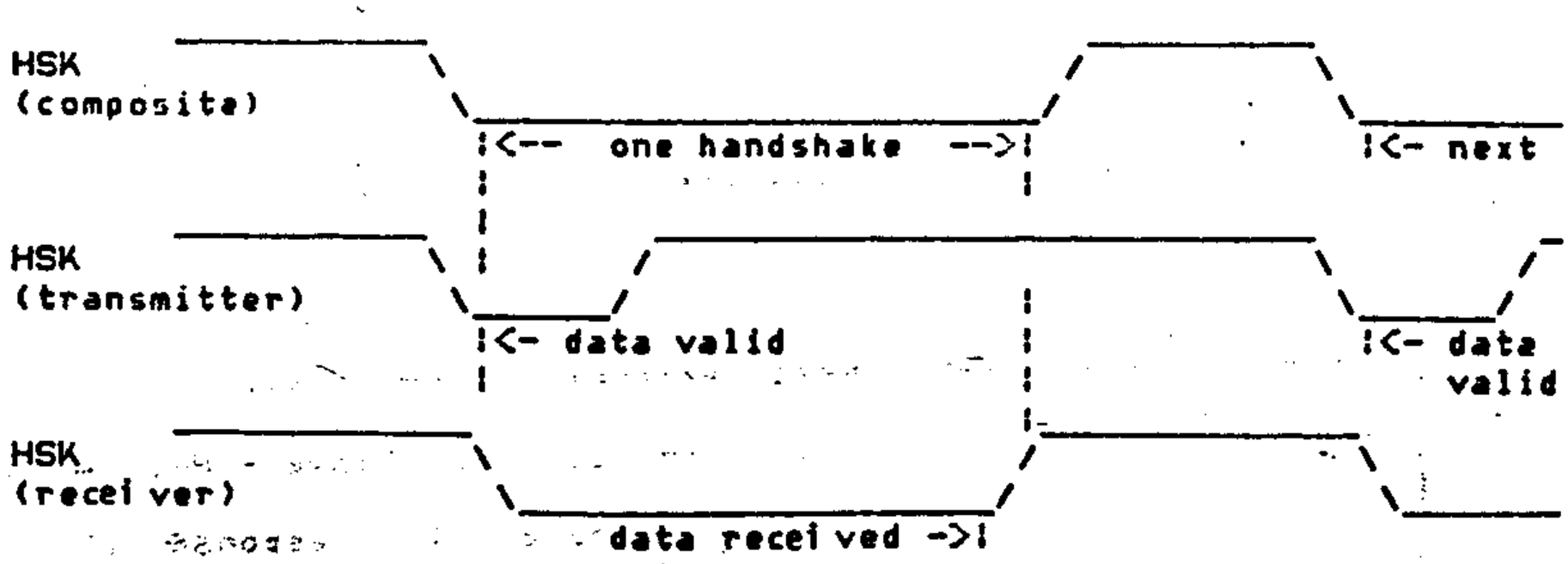
* BECAUSE DATA IS OUTPUT VIA OPEN DRAIN BUFFERS, DATA MUST BE SET HIGH ON THE RISING EDGE OF HSK.

** WITHIN A MESSAGE (WHEN BAV IS HELD LOW) HSK HAS 20 MS TO GO LOW OR A BUS TIMEOUT (ERROR) CONDITION RESULTS.

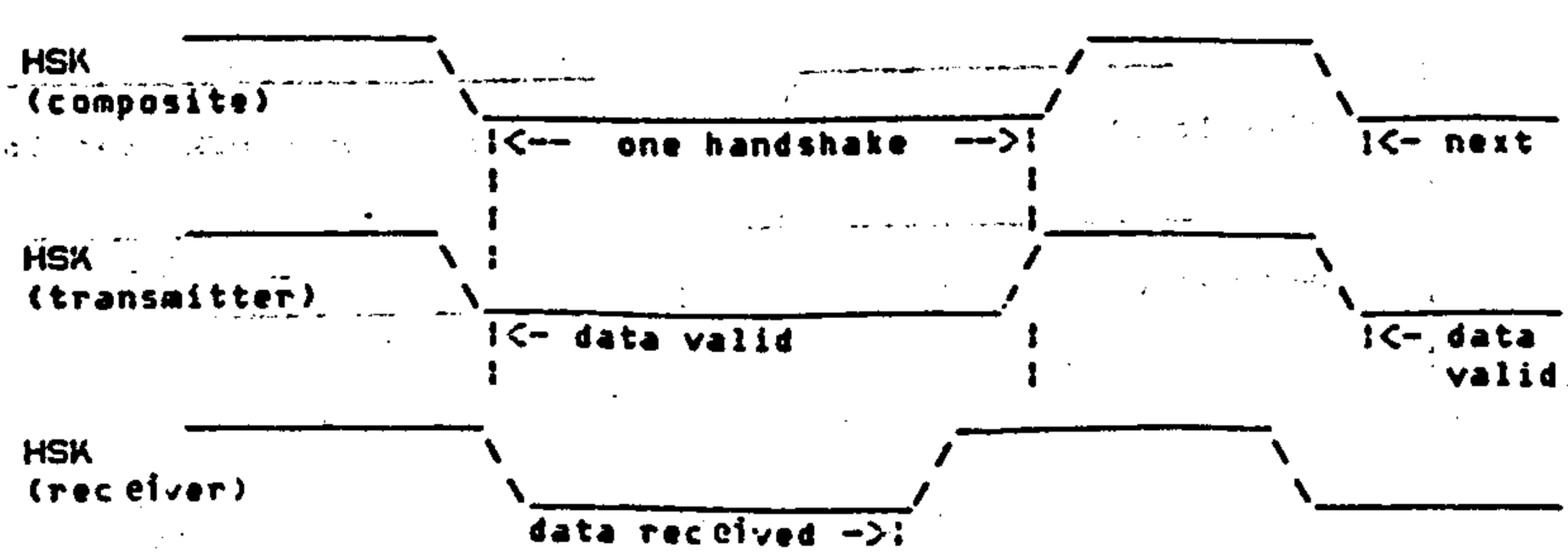
BUS HANDSHAKE TIMING



HANDSHAKE COMPONENTS - SLOW RECEIVER



HANDSHAKE COMPONENTS - SLOW TRANSMITTER



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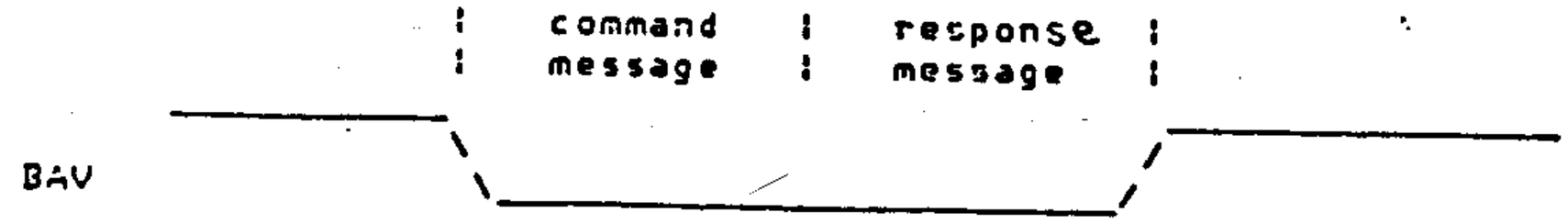
HEX BUS SPECIFICATION — TIMING CHARACTERISTICS

BAV TIMING PARAMETERS

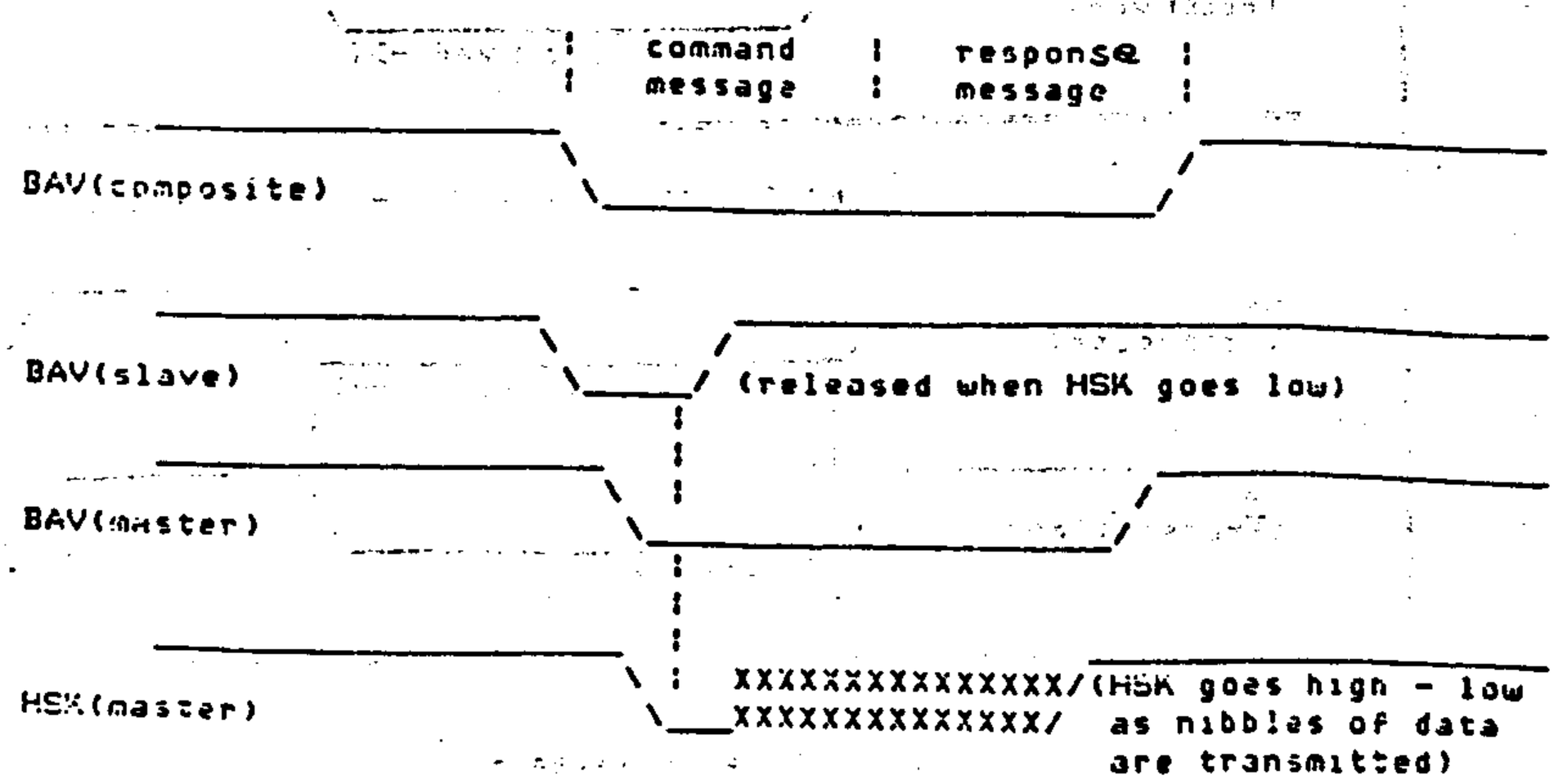
ITEM	MIN.(uSEC)	MAX.(uSEC)
BAV LOW TO HSK LOW	5	20,000
HSK HIGH TO BAV HIGH	1	--
END OF COMMAND TO START OF RESPONSE	10	--
HSK HIGH TO HSK LOW	8	20,000
BAV LOW(SLAVE) TO BAV HIGH(SLAVE)	**	SEE NOTE **
BAV HIGH TO BAV LOW(SLAVE)	2000**	--

** THESE TWO TIMING PARAMETERS OCCUR ONLY WHEN A SLAVE PERIPHERAL POLLS THE MASTER (BY PULLING BAV LOW) AT THE SAME TIME THE MASTER BAV GOES LOW. THE SLAVE WILL THEN CONTINUE TO HOLD BAV LOW UNTIL IT RECEIVES THE FIRST HSK SIGNAL FROM THE MASTER. THE SLAVE WILL THEN RELEASE BAV AND WAIT TWO MILLISECONDS AFTER THE MASTER HAS RELEASED BAV TO POLL AGAIN.

BAV Timing -- Polled by Master



BAV Timing -- Polled by Slave - Held by Master



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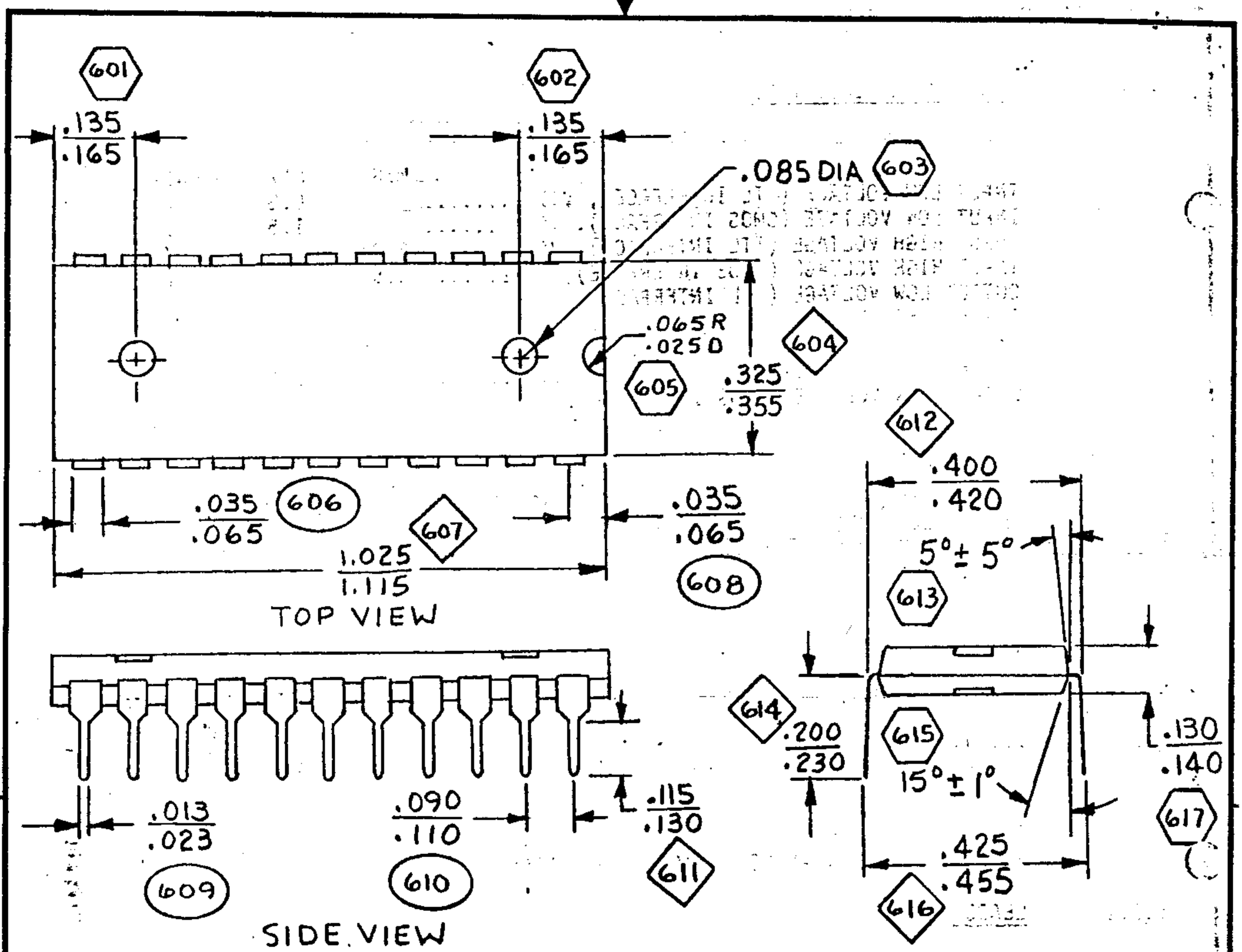

FIGURE 1. PACKAGE OUTLINE

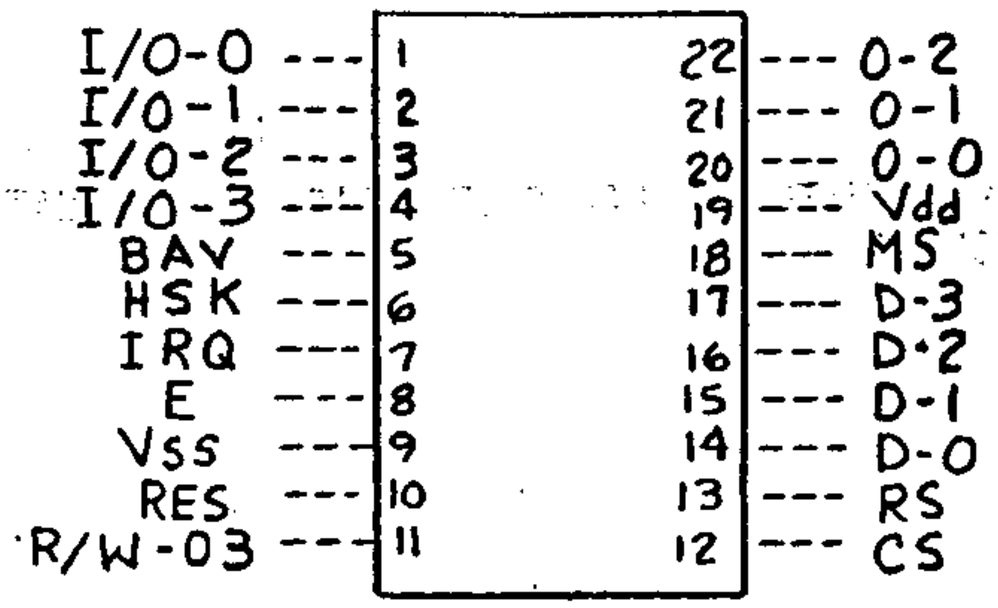

FIGURE 2. PIN CONFIGURATION

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6.0 PIN ASSIGNMENT FUNCTIONS:

NAME	PIN	I/O	DESCRIPTION
D-0	14	I/O	DATA I/O LINES THAT ALLOW DATA TRANSFER BETWEEN IBC AND ALC I/O BUS.
D-1	15	I/O	
D-2	16	I/O	
D-3	17	I/O	
HSK	6	I/O	HANDSHAKE LINE: SET LOW BY SOURCE DEVICE TO INDICATE TO LISTENERS THAT THERE IS VALID DATA ON THE ALC I/O BUS AND HELD LOW BY THE LISTENERS UNTIL THEY ACCEPT THE DATA.
BAV	5	I/O	BUS AVAILABLE LINE: SET LOW BY SOURCE DEVICE IN THE BEGINNING OF THE MESSAGE AND HELD LOW UNTIL THE END OF THE MESSAGE. THE NEW SOURCE CAN ORIGINATE A NEW MESSAGE OR "REQUEST SERVICE" ONLY IF THIS LINE IS HIGH.
I/O-0	1	I/O	DATA I/O LINES THAT ALLOW DATA TRANSFER BETWEEN IBC AND THE MICROPROCESSOR. IF MS = 1 LINES ACT AS INPUTS ONLY.
I/O-1	2	I/O	
I/O-2	3	I/O	
I/O-3	4	I/O	
IRQ	7	O	INTERRUPT OUTPUT (OPEN DRAIN): INDICATES TO THE MICROPROCESSOR THE OCCURANCE OF THE NEXT DATA NIBBLE ON THE ALC I/O BUS.
CS	12	I	CHIP SELECT INPUT: SELECTS AND ENABLES THE IBC FOR MICROPROCESSOR DATA TRANSFER.
RS	13	I	REGISTER SELECT INPUT: ADDRESS LINE THROUGH WHICH THE IBC REGISTERS CAN BE ACCESSED BY THE MICROPROCESSOR. WHEN IBC OPERATES IN THE LATCHED MODE THIS INPUT WORKS AS ADDRESS STROBE.
E	8	I	ENABLE INPUT: IF MS=0 THERE ARE SEVERAL OPTIONS IN COMBINATION WITH A PIN R/W FOR CONTROLLING DATA TRANSFER BETWEEN IBC AND THE MICROPROCESSOR. IF MS=1, E IS USED AS ACTIVE LOW STROBE FOR WRITING DATA INTO IBC.
R/W (0-3)	11	I/O	READ-WRITE CONTROL: IF MS=0 THERE ARE SEVERAL OPTIONS IN COMBINATION WITH A PIN E FOR CONTROLLING DIRECTION OF DATA TRANSFER BETWEEN IBC AND THE MICROPROCESSOR. IF MS=1, R/W IS USED AS MOST SIGNIFICANT BIT OF DATA OUTPUTS.
0-0	20,	I/O	OUTPUT DATA LINES: IF MS=1 THESE LINES ARE USED AS THREE LEAST SIGNIFICANT BITS OF DATA OUTPUTS. IF MS=0 THESE LINES ARE USED FOR SELECTING THE OPTIONS FOR PINS R/W, E AND RS.
0-1	21,	I/O	
0-2	22	I/O	

6.0 PIN ASSIGNMENT FUNCTIONS CONTINUED:

NAME	PIN	I/O	DESCRIPTION
MS	18	I	MODE SELECT: INPUT WHICH SELECTS THE MODE OF OPERATION.
RES	10	I	RESET INPUT: LOW LEVEL ON THIS INPUT WILL PUT IBC INTO RESET STATE.
VDD	19	I	POSITIVE SUPPLY (3 - 7 VDC).
VSS	9	I	0 VOLT REFERENCE.

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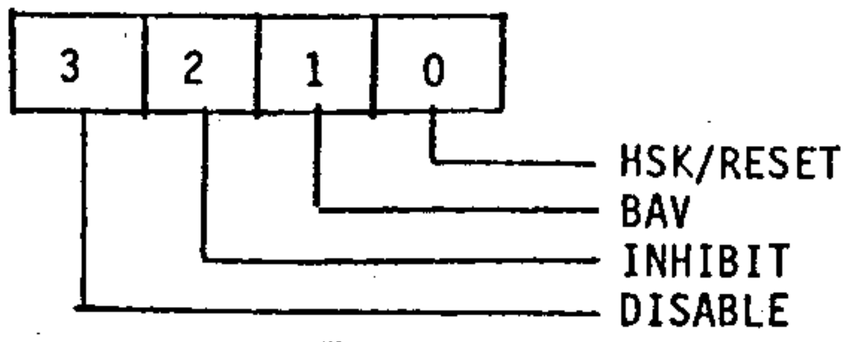
7.2.1 REGISTER DECODING:

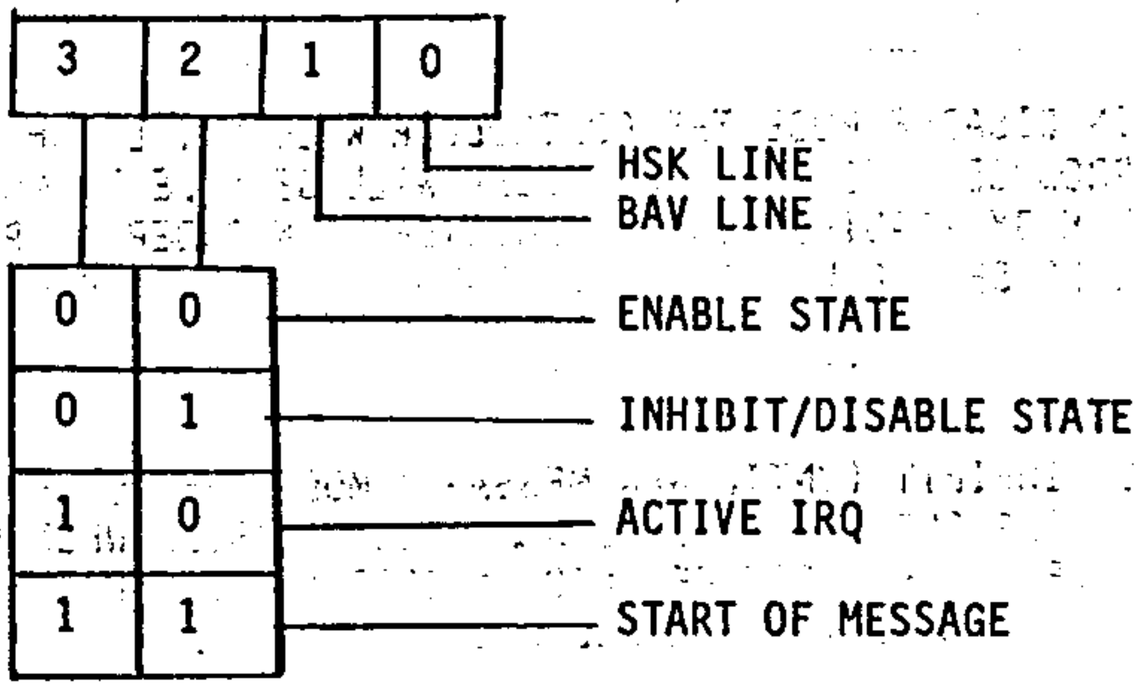
CS	RS	WRITE	READ
0	0	TRANSMIT DATA REGISTER	RECEIVER DATA REGISTER
0	1	CONTROL REGISTER	STATUS REGISTER

7.2.2 CONTROL REGISTER:



	3	2	1	0
HARDWARE RESET	1	1	0	0

7.2.3 STATUS REGISTER:



	3	2	1	0
HARDWARE RESET	0	1	X	X

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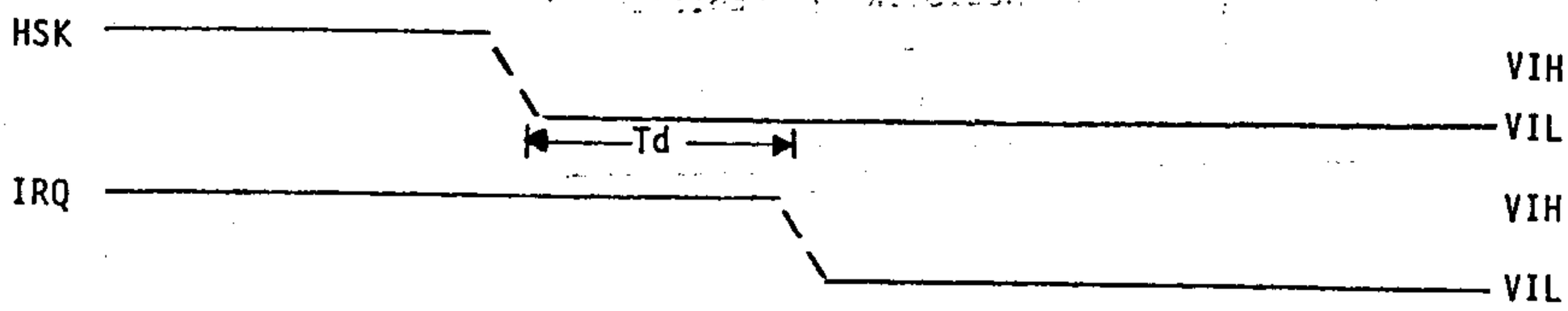
7.3 INTERRUPT:

THE IBC HAS AN INTERRUPT WHICH INDICATES WHEN THE DATA IS AVAILABLE ON THE BUS. INTERRUPT CAN BE DISABLED COMPLETELY OR UNTIL THE NEXT MESSAGE. THE INTERRUPT OUTPUT IS OPEN DRAIN WITH A LOW ACTIVE LEVEL. THE PULL-UP REGISTER VALUE IS BETWEEN 3.3K AND 4.7K OHMS.

7.3.1 INTERRUPT AC CHARACTERISTICS:



Td.....IRQ ACTIVE AFTER HSK FALL.....200ns (MAX)

8.0 FUNCTIONAL OPERATION DESCRIPTION:

8.1 POWER-UP CONSIDERATIONS:

IF SYSTEM'S POWER UP RESET IS TIED TO THE RESET PIN ON IBC, THE CONTROLLER WILL COME UP IN THE DISABLE STATE WHICH MEANS THAT TRANSITIONS ON HSK LINE WILL NOT BE LATCHED AND NO INTERRUPT WILL BE GENERATED. IN ORDER TO ENABLE THE CONTROLLER, THE USER HAS TO WRITE "0000" INTO CONTROL REGISTER. HOWEVER IT MIGHT NOT BE DESIRABLE TO ENABLE THE CONTROLLER IN THE MIDDLE OF THE MESSAGE THEREFORE USER MAY PERFORM ENABLE WITH "INHIBIT UNTIL NEW MESSAGE" BY WRITING "0100" INTO CONTROL REGISTER. THIS WILL KEEP THE CONTROLLER IN DISABLE STATE UNTIL A NEW MESSAGE STARTS.

8.2 DISABLE MODE:

IN DISABLE MODE THE CONTROLLER WILL NOT LATCH HSK SIGNAL AND WILL NOT PRODUCE INTERRUPT, BUT USER WILL BE ABLE TO MONITOR STATE OF BAV AND HSK BY READING STATUS REGISTER. IN ORDER TO PUT DEVICE IN DISABLE MODE USER SHOULD WRITE "1100" INTO THE CONTROL REGISTER.

8.3 INHIBIT (UNTIL NEW MESSAGE):

IN INHIBIT (UNTIL NEW MESSAGE) MODE THE CONTROLLER WILL BE DISABLED DURING CURRENT MESSAGE AND FULLY ENABLED WHEN NEXT MESSAGE STARTS. IN ORDER TO PUT DEVICE INTO INHIBIT (UNTIL NEW MESSAGE) USER SHOULD WRITE "0100" INTO THE CONTROL REGISTER.

8.4 LISTEN MODE:

IN LISTEN MODE THE USER HAS TO READ THE FIRST TWO NIBBLES ON THE BUS, DETERMINE IF HE WAS SELECTED, AND IF HE WAS, THE USER CAN START COMMUNICATION WITH THE MASTER. IF HE WAS NOT SELECTED THE USER SHOULD PERFROM "INHIBIT UNTIL NEW MESSAGE" BY WRITING "0100" INTO THE CONTROL REGISTER.

8.5 MONITOR MODE:

THE CAPABILITY EXISTS FOR USER TO MONITOR THE COMMUNICATION EVEN IF HE WAS NOT SELECTED, HOWEVER, THIS IS NOT RECOMMENDED SINCE IT MAY SLOW DOWN THE BUS OPERATION. THIS CAPABILITY ALLOWS MONITORING AND RECORDING OF ALL BUS COMMUNICATIONS.

8.6 TRANSMIT MODE:

IN TRANSMIT MODE, THE USER HAS TO SEND THE DATA UTILIZING THE WRITE SEQUENCE, MONITOR THE HSK LINE AND WHEN THE HSK LINE GOES INTO AN INACTIVE STATE THE USER MAY TRANSMIT THE NEXT DATA.

8.7 DATA TRANSFER OPERATION:

ALL RECEIVE AND TRANSMIT DATA CAN BE HANDLED BY EXECUTING THE READ AND WRITE SEQUENCES RESPECTIVELY.

8.7.1 READ SEQUENCE:

THE READ SEQUENCE ALLOWS THE USER TO OBTAIN THE DATA TRANSMITTED ON THE BUS AND PREPARES IBC TO RECEIVE THE NEXT TRANSMISSION. THE READ SEQUENCE HAS TO BE USED WHENEVER THE USER IS IN THE LISTEN MODE AND RECEIVES AN INTERRUPT FROM IBC.

A - RESET INTERRUPT - WRITE "0001" INTO CONTROL REGISTER
B - OBTAIN DATA - READ RECEIVER DATA REGISTER
C - RESET HSK LATCH - WRITE "0000" INTO CONTROL REGISTER

8.7.2 WRITE SEQUENCE:

THE WRITE SEQUENCE ALLOWS THE USER TO PLACE THE DATA ON THE BUS AND TO SIGNAL THE OTHER DEVICES THAT THE DATA IS AVAILABLE. THE WRITE SEQUENCE HAS TO BE USED WHENEVER THE USER IS IN TRANSMIT MODE AND READY TO SEND THE DATA.

A - PREPARE DATA - WRITE DATA INTO TRANSMIT DATA REGISTER
B - SET HSK SIGNAL - WRITE "0001" INTO CONTROL REGISTER
C - RESET HSK SIGNAL - WRITE "0000" INTO CONTROL REGISTER

8.8 REQUEST SERVICE SEQUENCE:

THE REQUEST SERVICE SEQUENCE ALLOWS THE USER TO SIGNAL THE MASTER BY PUTTING THE BAV LINE INTO THE LOW STATE UNTIL THE FIRST HSK TRANSITION. THE REQUEST SERVICE SEQUENCE MAY BE USED WHENEVER THE USER HAS PERMISSION FROM THE MASTER TO REQUEST THE SERVICE.

A - SET BAV SIGNAL - WRITE "0010" INTO CONTROL REGISTER
B - ENABLE BAV RESET - WRITE "0000" INTO CONTROL REGISTER

8.9 MASTER MODE DIFFERENCES:

THE DIFFERENCE BETWEEN MASTER AND SLAVE MODES OF OPERATION EXISTS BECAUSE IN MASTER MODE THE USER HAS TO HOLD THE BAV LINE LOW DURING THE ENTIRE MESSAGE. THEREFORE THE READ AND WRITE SEQUENCES SHOWN ABOVE MUST BE MODIFIED FOR MASTER MODE OPERATION. THE MODIFICATION REQUIRES THAT ALL ACCESSES TO THE CONTROL REGISTER MUST MAINTAIN THE BAV BIT IN THE HIGH STATE.

9.0 MODES OF OPERATION:

THE IBC CAN OPERATE IN 7 DIFFERENT MODES WHICH ALLOWS SIMPLE INTERFACE WITH SEVERAL POPULAR MICROPROCESSORS FAMILIES. THE DESIRED MODE CAN BE SELECTED BY SETTING THE MODE SELECT INPUT (MS). IF INPUT MS IS SET LOW THREE MODES CAN BE SELECTED BY SETTING PINS O-O AND O-1. TABLE 1 SHOWS THE MODES SELECTED BY DIFFERENT BIT PATTERNS ON THESE PINS.

IN ADDITION, WHEN MS IS SET LOW, SETTING PIN O-2 WILL ENABLE THE LATCHING CAPABILITY FOR CS AND RS SIGNALS. THIS FEATURE IS USEFUL FOR MULTIPLEX ADDRESS/DATA BUS SILIMAR TO TMS-7000 OR INTEL-8085. IN THIS MODE ALATCH IS CONNECTED TO THE RS PIN AND A POSITIVE STROBE ON ALATCH WILL LATCH THE LEVEL ON I/O-O PIN AS INTERNAL RS AND THE LEVEL ON CS PIN AS INTERNAL CS WHICH SHOULD BE HIGH TO SELECT THE CHIP.

IF THE MS IS SET HIGH THE IBC IS IN MODE 7 AND RECONFIGURED AS SHOWN IN SECTION 9.7. THIS MODE IS USEFUL WITH 4-BIT MPUs WHICH DON'T HAVE A BIDIRECTIONAL BUS. PLEASE NOTE THAT PIN R/W IS USED AS MSB OF THE OUTPUT DATA.

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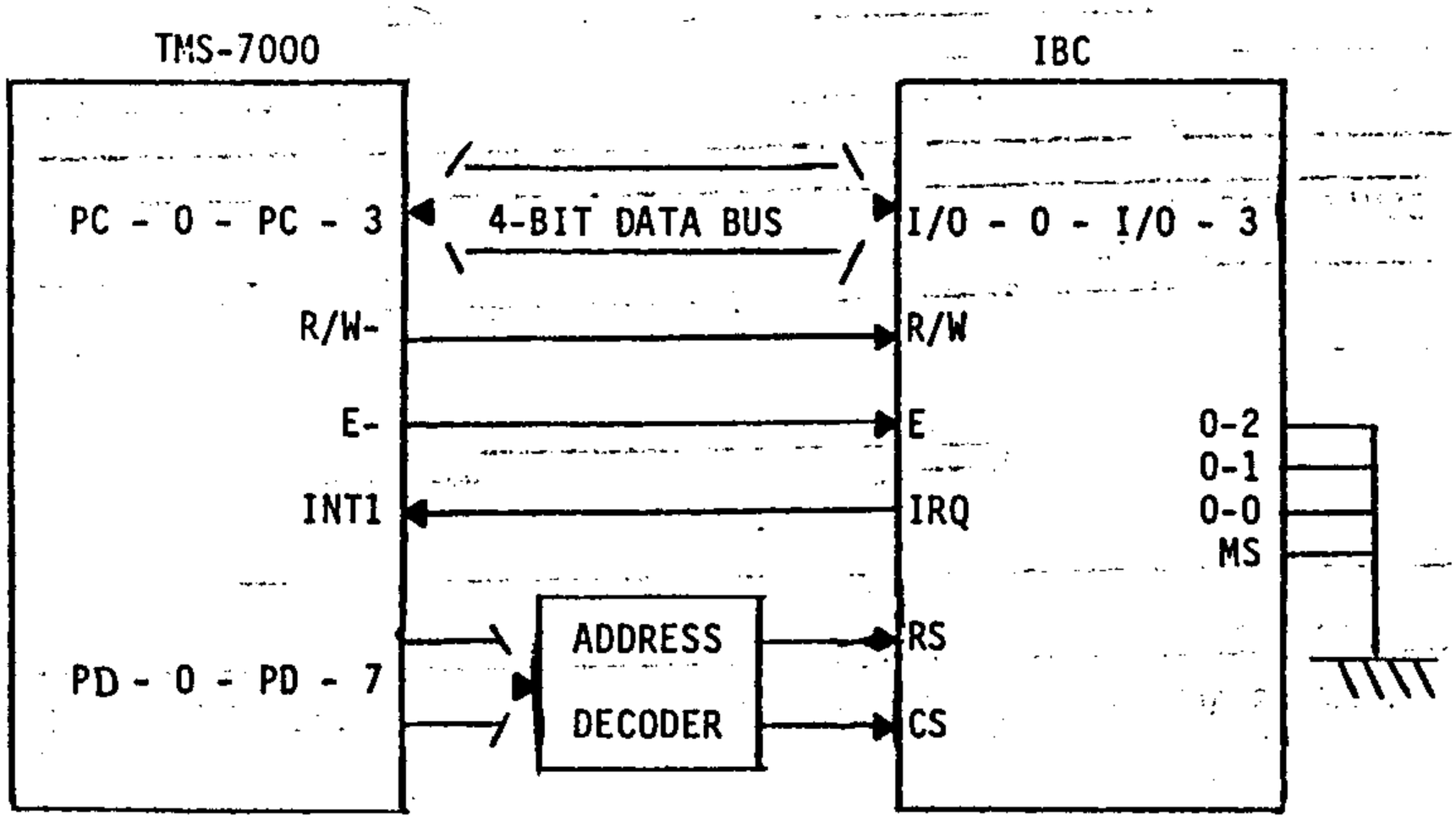
9.0 MODES OF OPERATION (CONTINUED):

TABLE 1. MODES OF OPERATION.

0-2	0-1	0-0	MODE DESCRIPTION
0	0	0	MODE 0 - ENABLE ACTIVE LOW (SEE FIGURE 3) TMS-7000 COMPATIBLE
0	0	1	MODE 1 - ENABLE ACTIVE HIGH (SEE FIGURE 4) 6500 COMPATIBLE
0	1	0	MODE 2 - ACCEPTS RD- AND WR- SIGNALS (SEE FIGURE 5) 8085 AND 8048 COMPATIBLE
1	X	X	MODES 4, 5, 6 - CONTROL SIGNALS FOR R/W AND E CORRESPOND TO NON-MULTIPLEX MODES 0, 1, 2 BUT ADDRESSING ARRANGED FOR MULTIPLEX BUSSES.

9.1 MODE 0 SPECIFICATIONS:

9.1.1 MODE 0 INTERFACE CONFIGURATION:



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A		1052911
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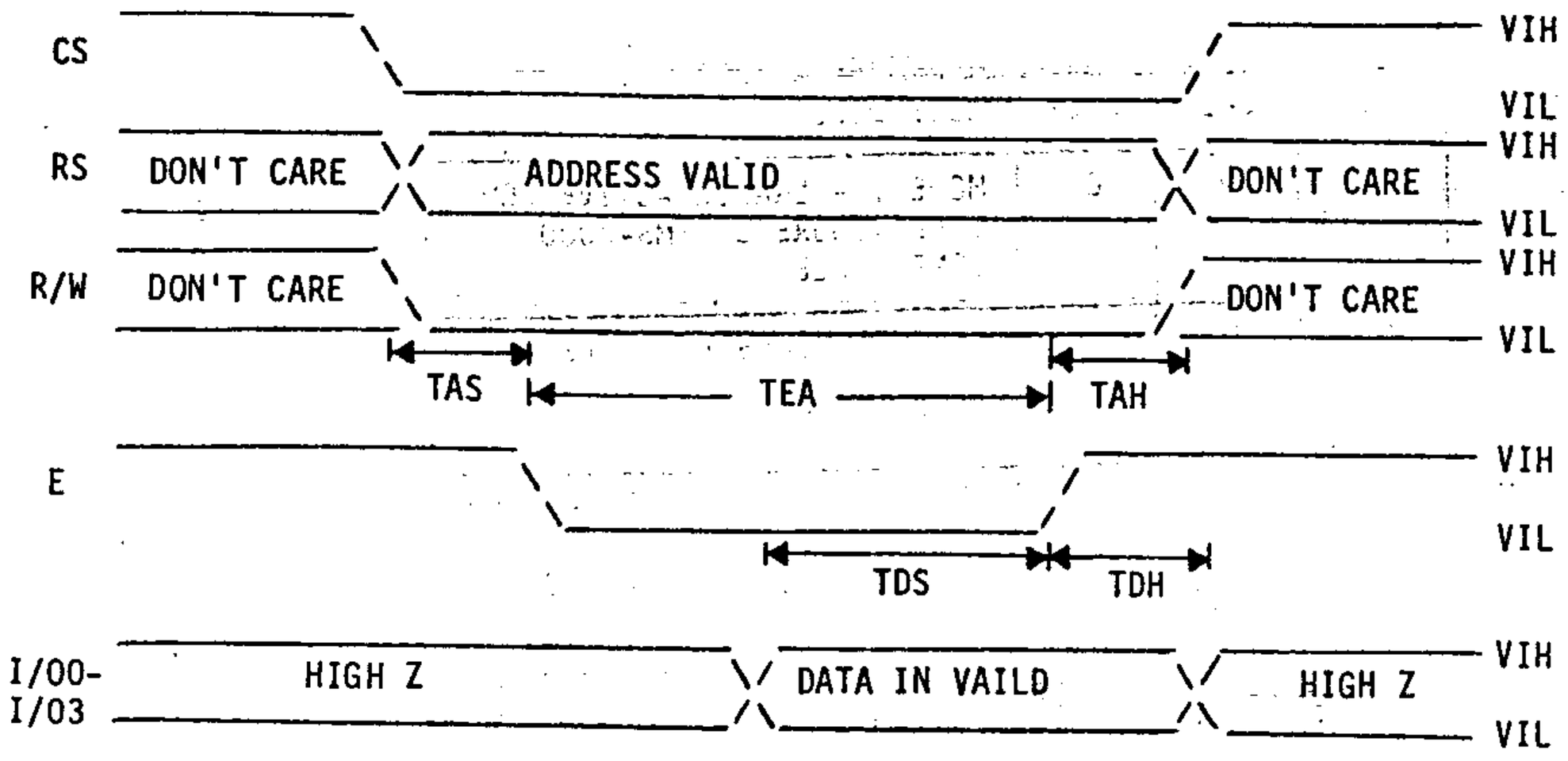
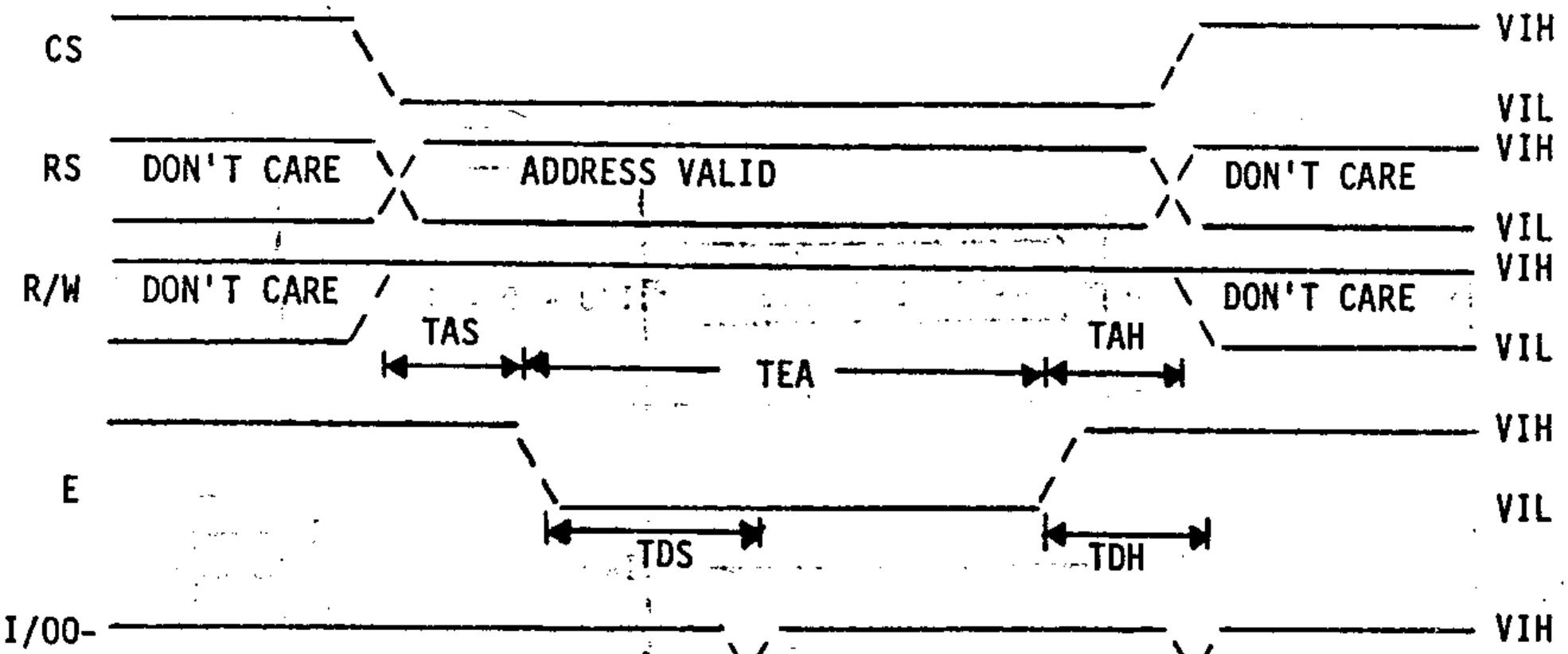
9.1.2 MODE 0 WRITE SEQUENCE AC CHARACTERISTICS:



TAS.....ADDRESS AND R/W VALID BEFORE E FALL..... 50 NS (MIN)
TAH.....ADDRESS AND R/W HOLD VALID AFTER E RISE..... 30 NS (MIN)
TDS.....DATA IN VALID BEFORE E RISE.....150 NS (MIN)
TDH.....DATA IN HOLD VALID AFTER E RISE..... 65 NS (MIN)
TEA.....ENABLE ACTIVE.....300 NS (MIN)

9.1.3 MODE 0 READ SEQUENCE AC CHARACTERISTICS:



TAS.....ADDRESS AND R/W VALID BEFORE E FALL..... 50 NS (MIN)
TAH.....ADDRESS AND R/W HOLD VALID AFTER E RISE..... 30 NS (MIN)
TDS.....DATA OUT VALID AFTER E FALL.....120 NS (MAX)
TDH.....DATA OUT HOLD VALID AFTER E RISE..... 60 NS (MAX)
TEA.....ENABLE ACTIVE.....300 NS (MIN)

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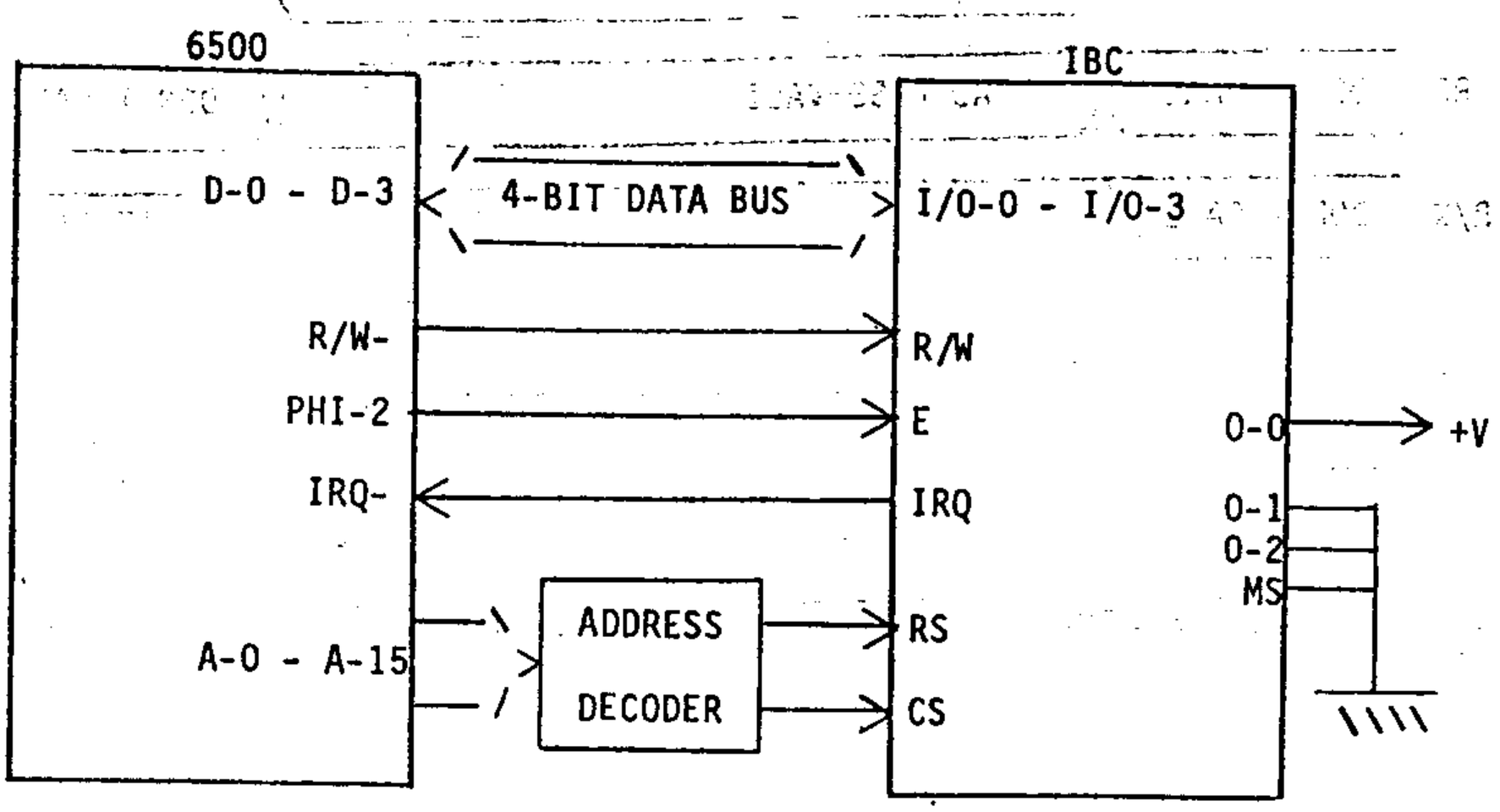
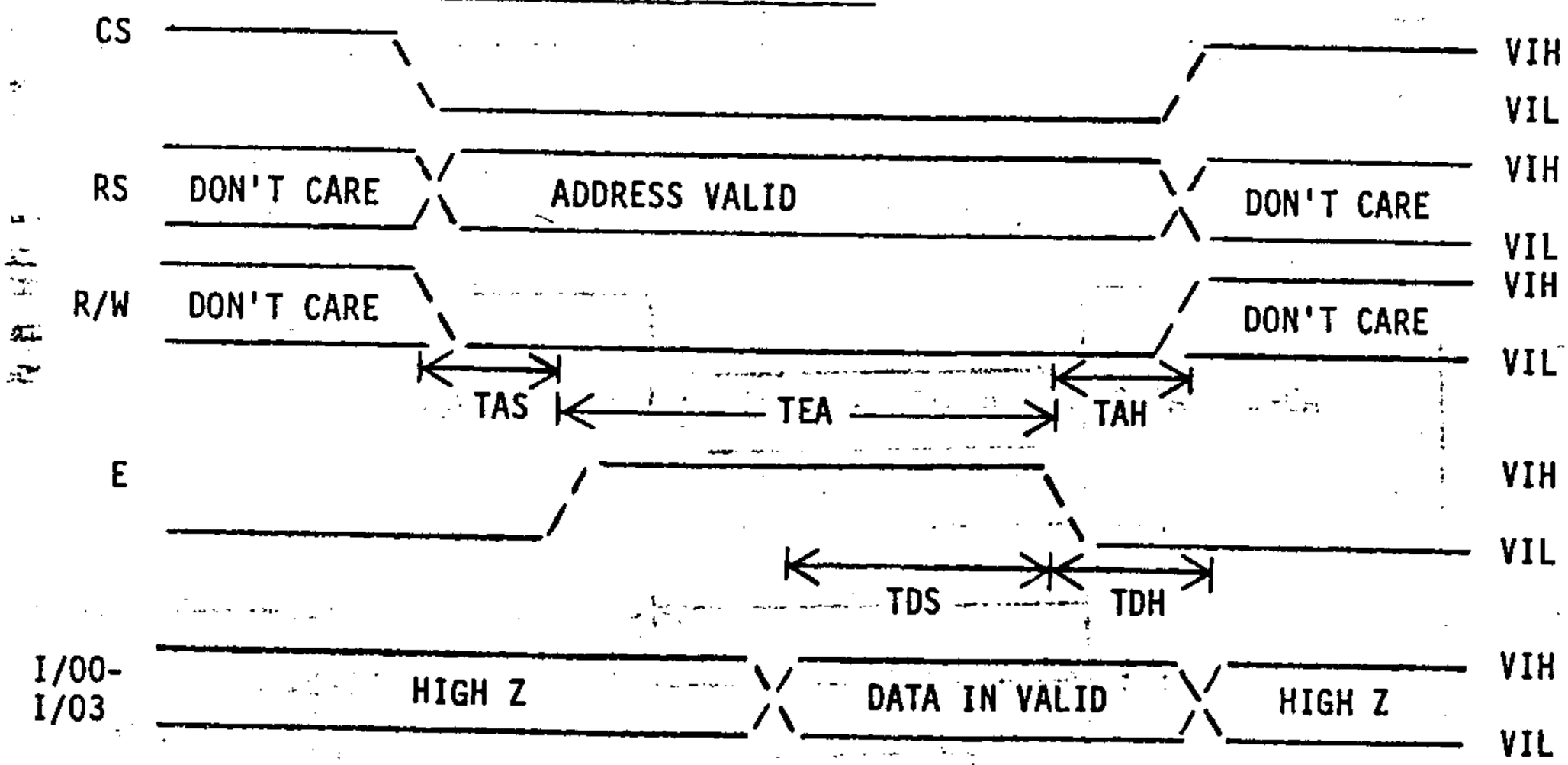
A		1052911
SCALE	REV A	SHEET 15

9.2 MODE 1 SPECIFICATIONS:

9.2.1 MODE 1 INTERFACE CONFIGURATION:



9.2.2 MODE 1 SEQUENCE AC CHARACTERISTICS:



TAS.....ADDRESS AND R/W VALID BEFORE E RISE..... 50 NS (MIN)
TAH.....ADDRESS AND R/W HOLD VALID AFTER E FALL..... 30 NS (MIN)
TDS.....DATA IN VALID BEFORE E FALL.....100 NS (MIN)
TDH.....DATA IN HOLD VALID AFTER E FALL..... 60 NS (MIN)
TEA.....ENABLE ACTIVE.....140 NS (MIN)

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A		1052911
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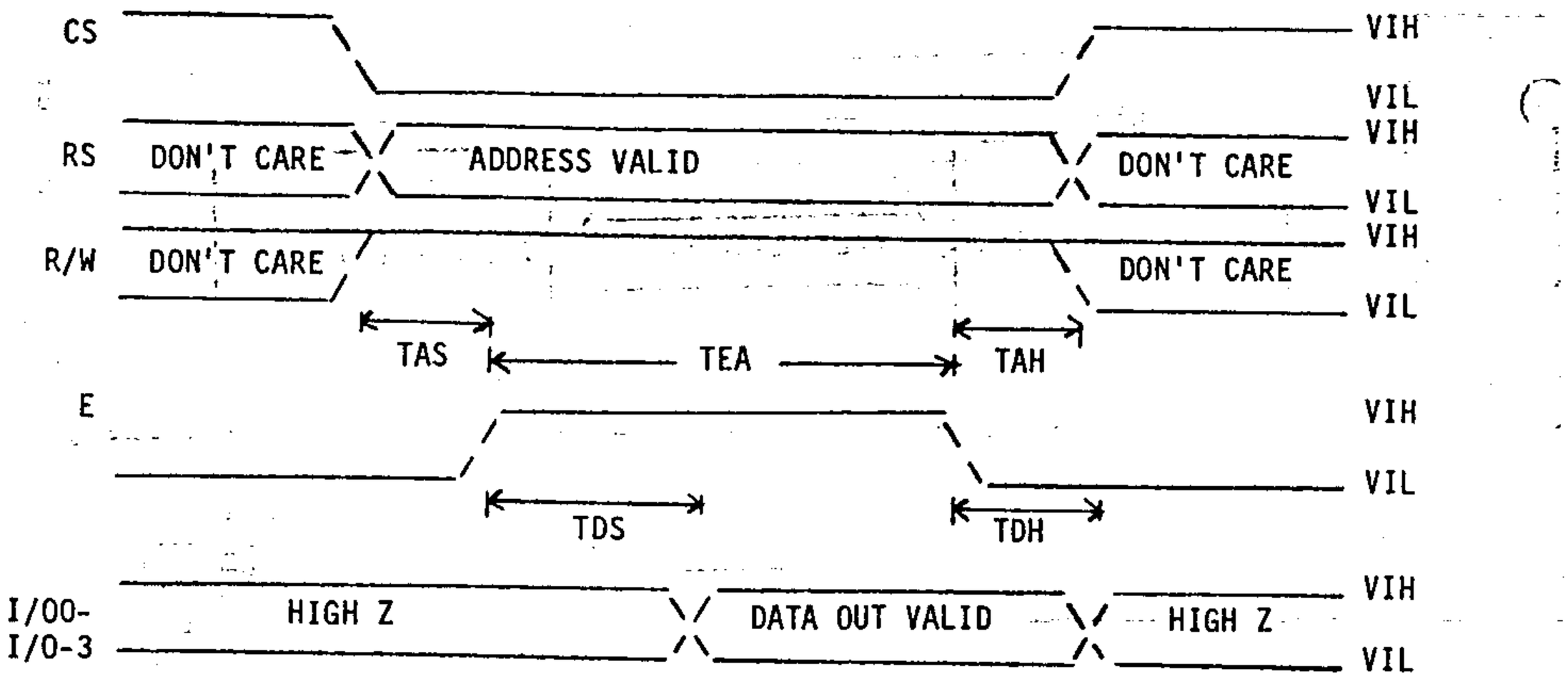
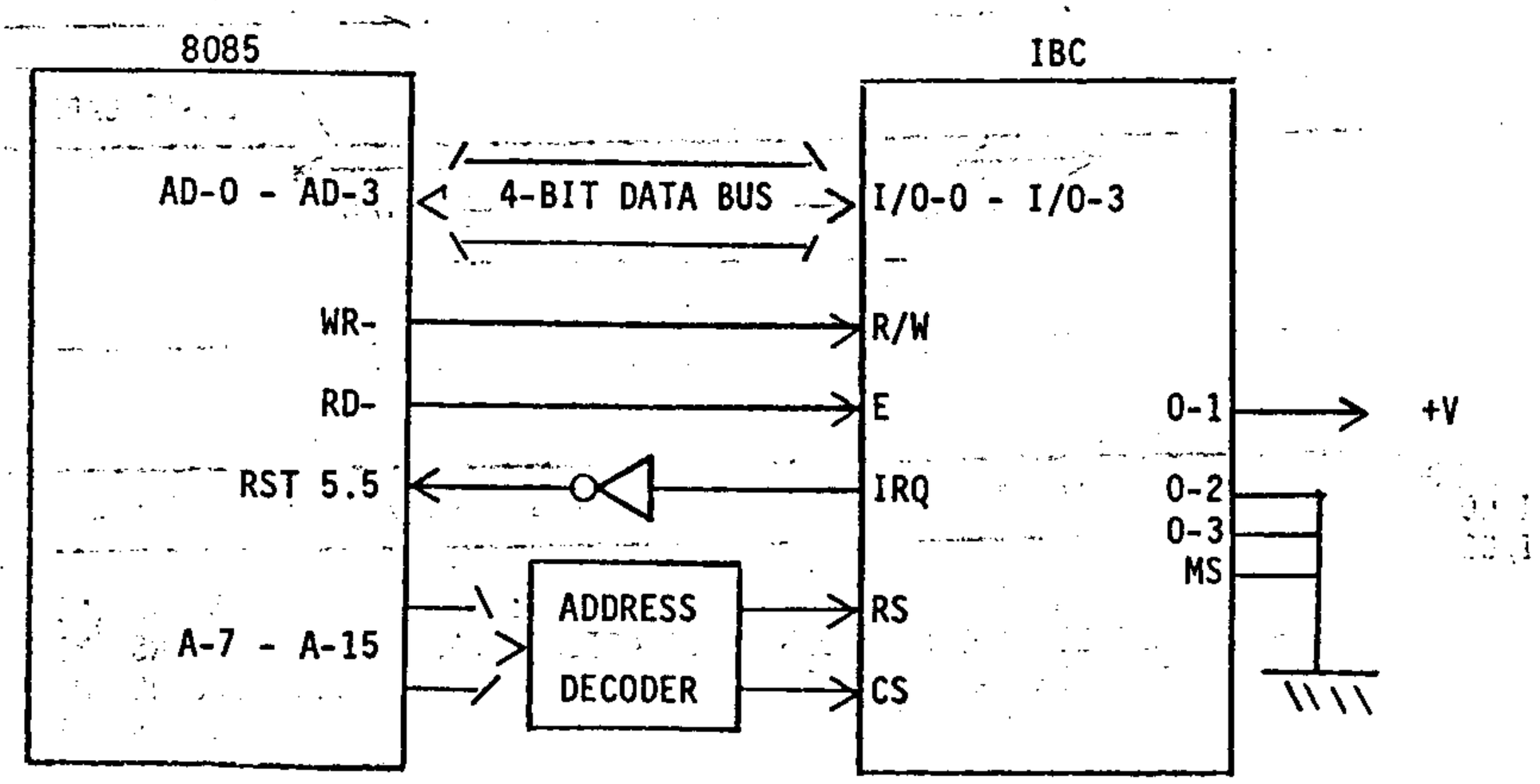
9.2.3 MODE 1 READ SEQUENCE AC CHARACTERISTICS:



TAS.....ADDRESS AND R/W VALID BEFORE E RISE..... 50 NS (MIN)
TAH.....ADDRESS AND R/W HOLD VALID AFTER E FALL..... 30 NS (MIN)
TDS.....DATA OUT VALID AFTER E RISE.....120 NS (MAX)
TDH.....DATA OUT HOLD VALID AFTER E FALL..... 60 NS (MAX)
TEA.....ENABLE ACTIVE.....140 NS (MIN)

9.3 MODE 2 SPECIFICATIONS:

9.3.1 MODE 2 INTERFACE CONFIGURATION:



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A		1052911
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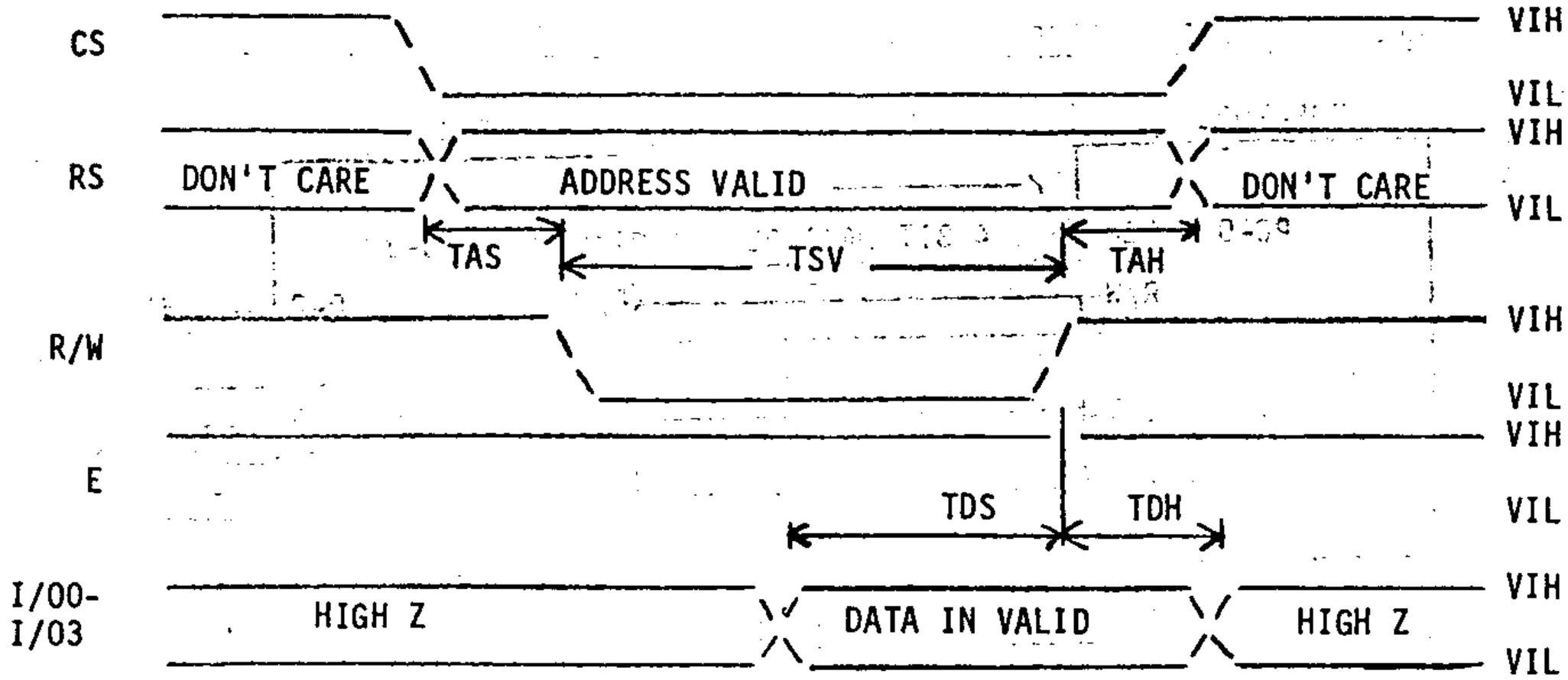
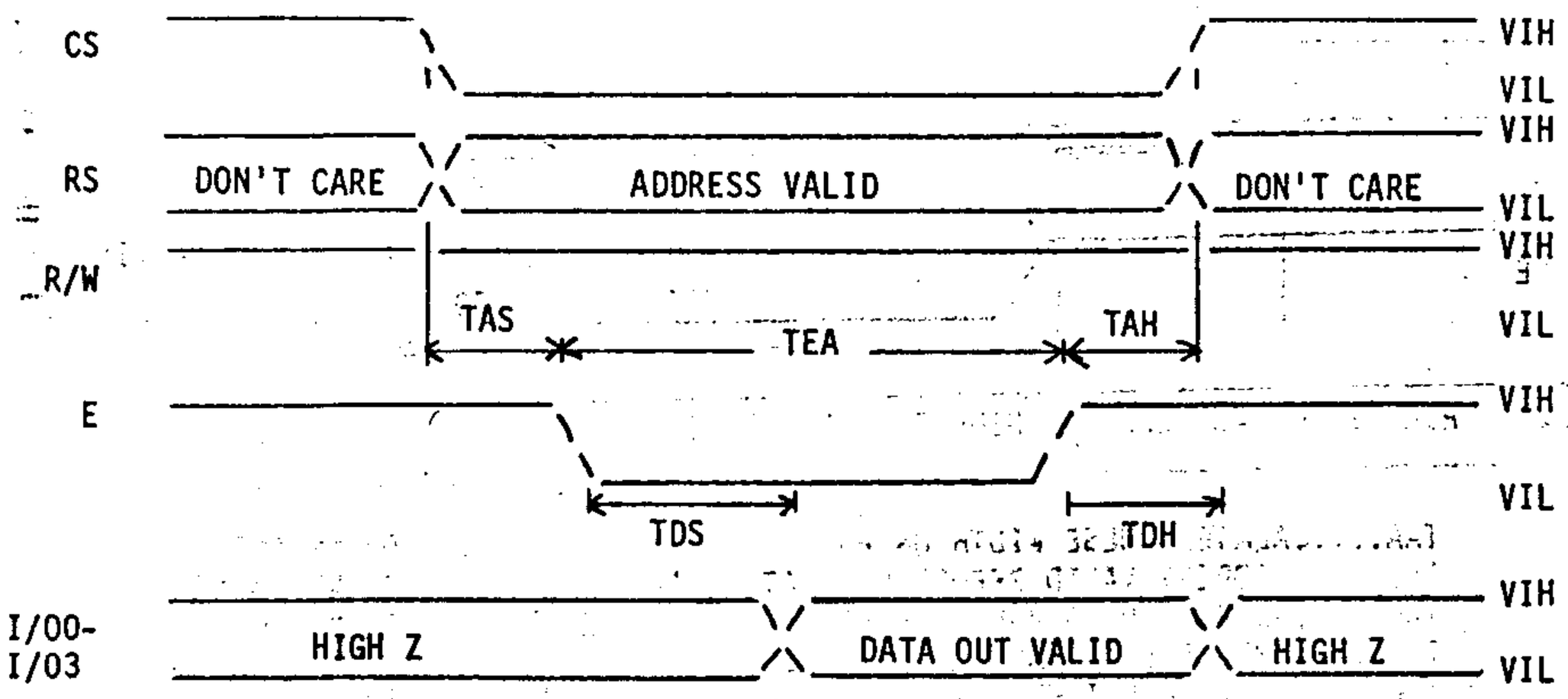
9.3.2 MODE 2 WRITE SEQUENCE AC CHARACTERISTICS:



TAS.....ADDRESS VALID BEFORE R/W FALL..... 50 NS (MIN)
TAH.....ADDRESS HOLD VALID AFTER R/W RISE..... 50 NS (MIN)
TDS.....DATA IN VALID BEFORE R/W RISE.....150 NS (MIN)
TDH.....DATA IN HOLD VALID AFTER R/W RISE..... 60 NS (MIN)
TSV.....WRITE PULSE WIDTH ON R/W PIN.....140 NS (MIN)

9.3.3 MODE 2 READ SEQUENCE AC CHARACTERISTICS:

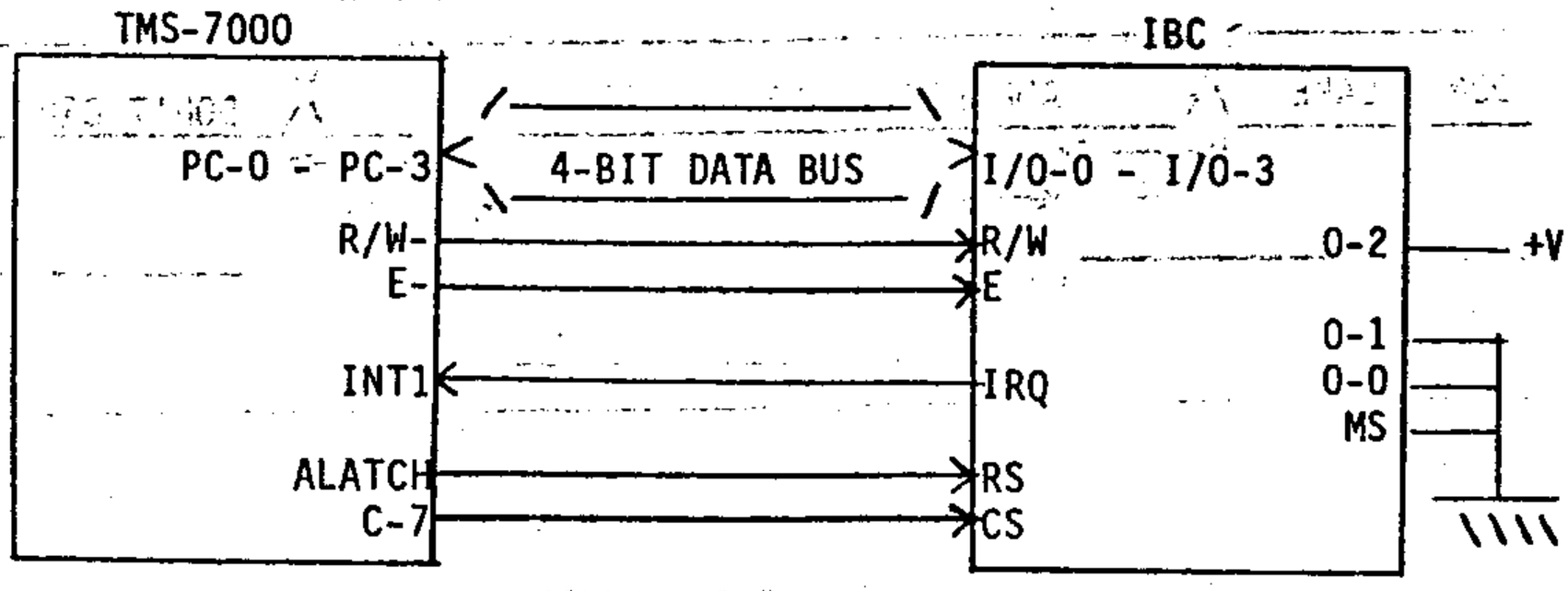


TAS.....ADDRESS VALID BEFORE E FALL..... 50 NS (MIN)
TAH.....ADDRESS HOLD VALID AFTER E RISE..... 50 NS (MIN)
TDS.....DATA OUT VALID AFTER E FALL.....120 NS (MAX)
TDH.....DATA OUT HOLD VALID AFTER E RISE..... 60 NS (MAX)
TEA.....READ PULSE WIDTH ON E PIN.....140 NS (MIN)

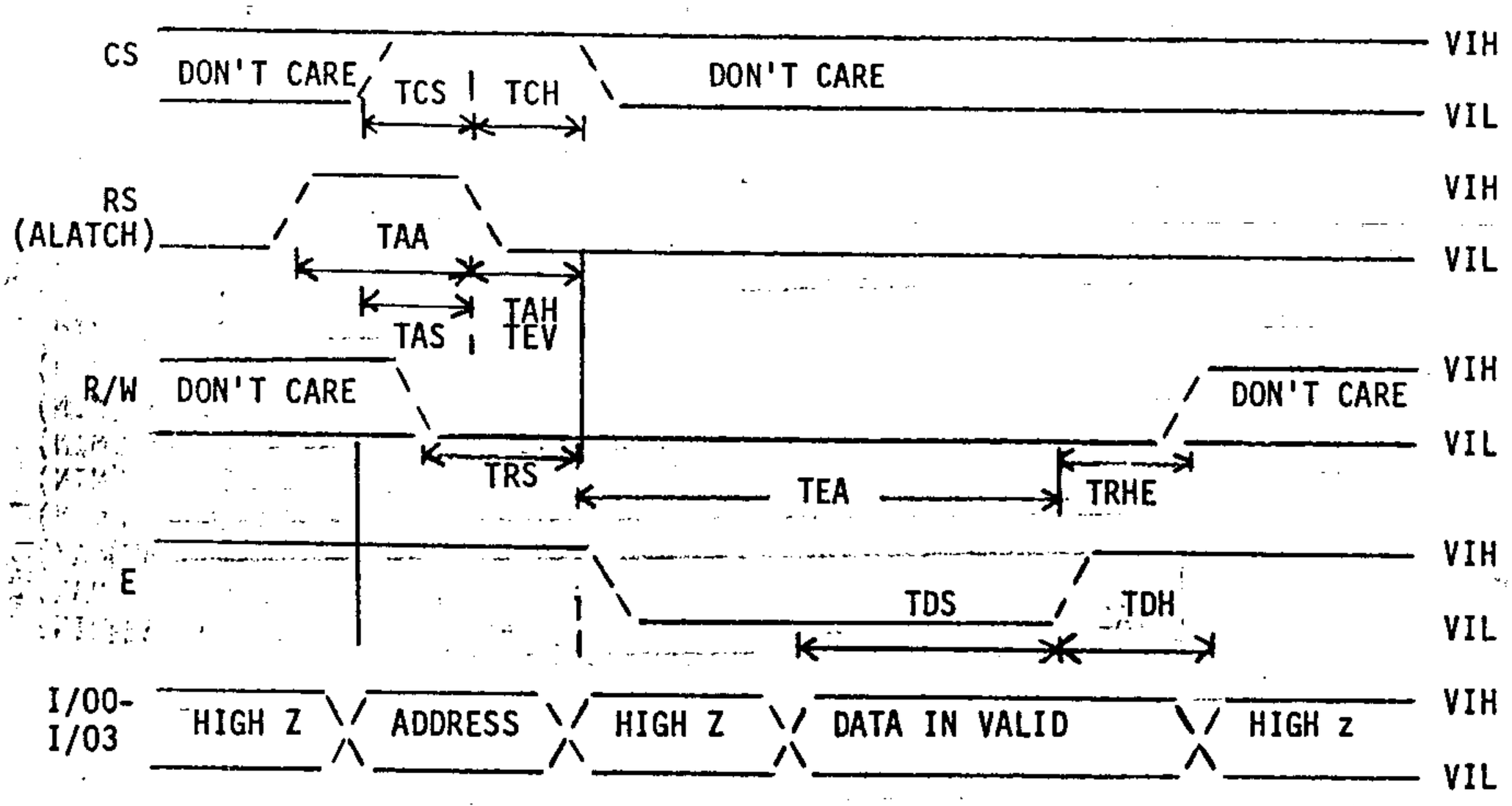
SIZE		DRAWING NO.
A		1052911
SCALE	REV A	SHEET 18

9.4 MODE 4 SPECIFICATIONS:

9.4.1 MODE 4 INTERFACE CONFIGURATION:

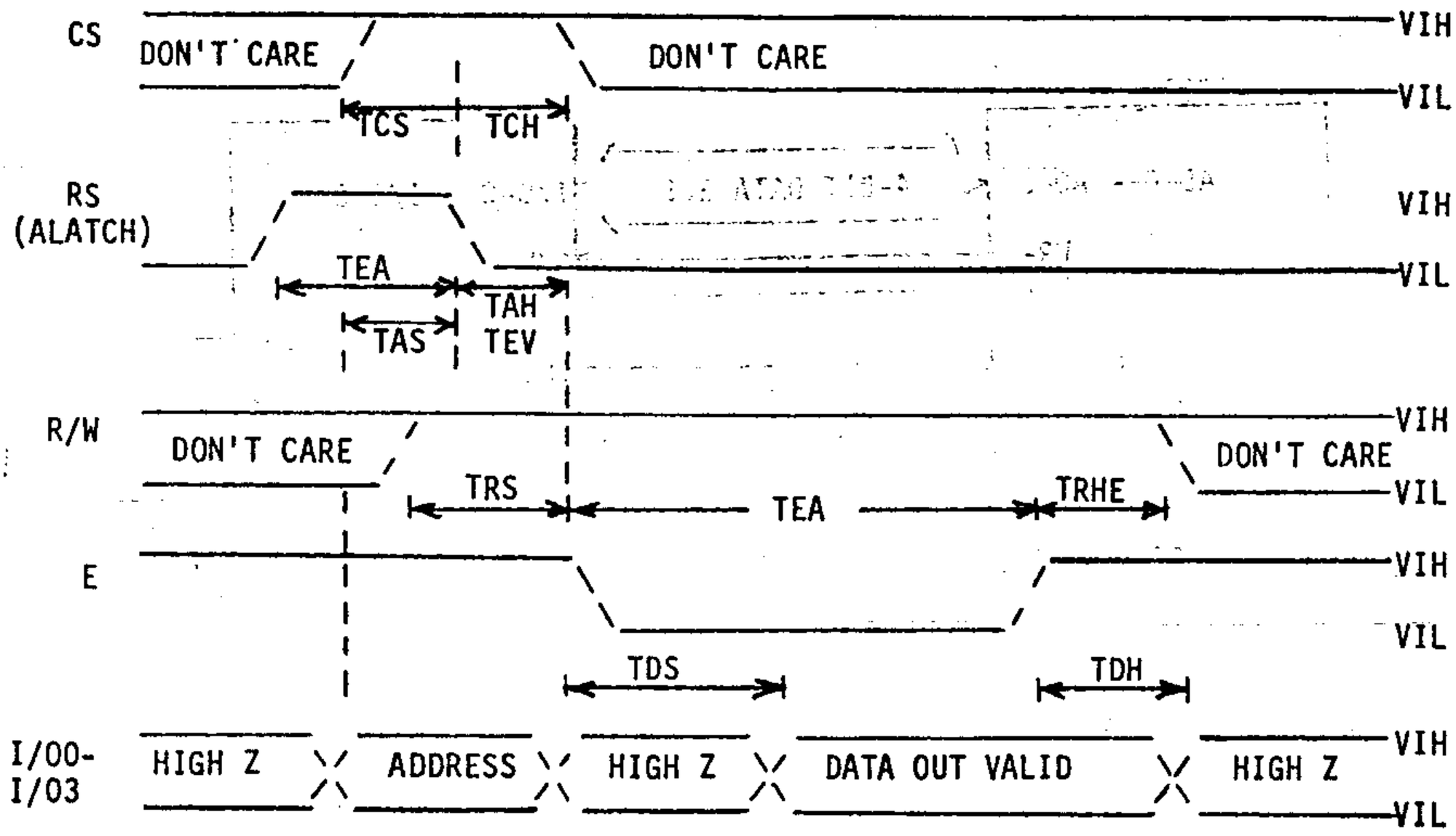


9.4.2 MODE 4 WRITE SEQUENCE AC CHARACTERISTICS:



TAA.....ALATCH PULSE WIDTH ON RS PIN.....100 NS (MIN)
TAS.....ADDRESS VALID BEFORE RS(ALATCH) FALL..... 30 NS (MIN)
TAH.....ADDRESS HOLD VALID AFTER RS(LATCH) FALL..... 30 NS (MIN)
TCS.....CHIP SELECT VALID BEFORE RS(LATCH) FALL..... 30 NS (MIN)
TCH.....CHIP SELECT HOLD VALID AFTER RS(LATCH) FALL... 30 NS (MIN)
TSV.....E VALID AFTER RS(LATCH) FALL..... 30 NS (MIN)
TRS.....R/W VALID BEFORE E FALL..... 30 NS (MIN)
TRH.....R/W HOLD VALID AFTER E RISE..... 30 NS (MIN)
TDS.....DATA IN VALID BEFORE E RISE.....150 NS (MIN)
TDH.....DATA IN HOLD VALID AFTER E RISE..... 65 NS (MIN)
TEA.....ENABLE ACTIVE.....250 NS (MIN)

9.4.3 MODE 4 READ SEQUENCE AC CHARACTERISTICS:



TAA....ALATCH PULSE WIDTH ON RS PIN.....100 MS (MIN)
TAS....ADDRESS VALID BEFORE RS(ALATCH) FALL..... 30 NS (MIN)
TAH....ADDRESS HOLD VALID AFTER RS(ALATCH) FALL..... 30 NS (MIN)
TCS....CHIP SELECT VALID BEFORE RS(ALATCH) FALL..... 30 NS (MIN)
TCH....CHIP SELECT HOLD VALID AFTER RS(ALATCH) FALL..... 30 NS (MIN)
TEV....E VALID AFTER RS(ALATCH) FALL..... 30 NS (MIN)
TRS....R/W VALID BEFORE E FALL..... 30 NS (MIN)
TRH....R/W HOLD VALID AFTER E RISE..... 30 NS (MIN)
TDS....DATA OUT VALID AFTER E FALL.....120 NS (MAX)
TDH....DATA OUT HOLD VALID AFTER E RISE.....60 NS (MAX)
TEA....ENABLE ACTIVE.....250 NS (MIN)

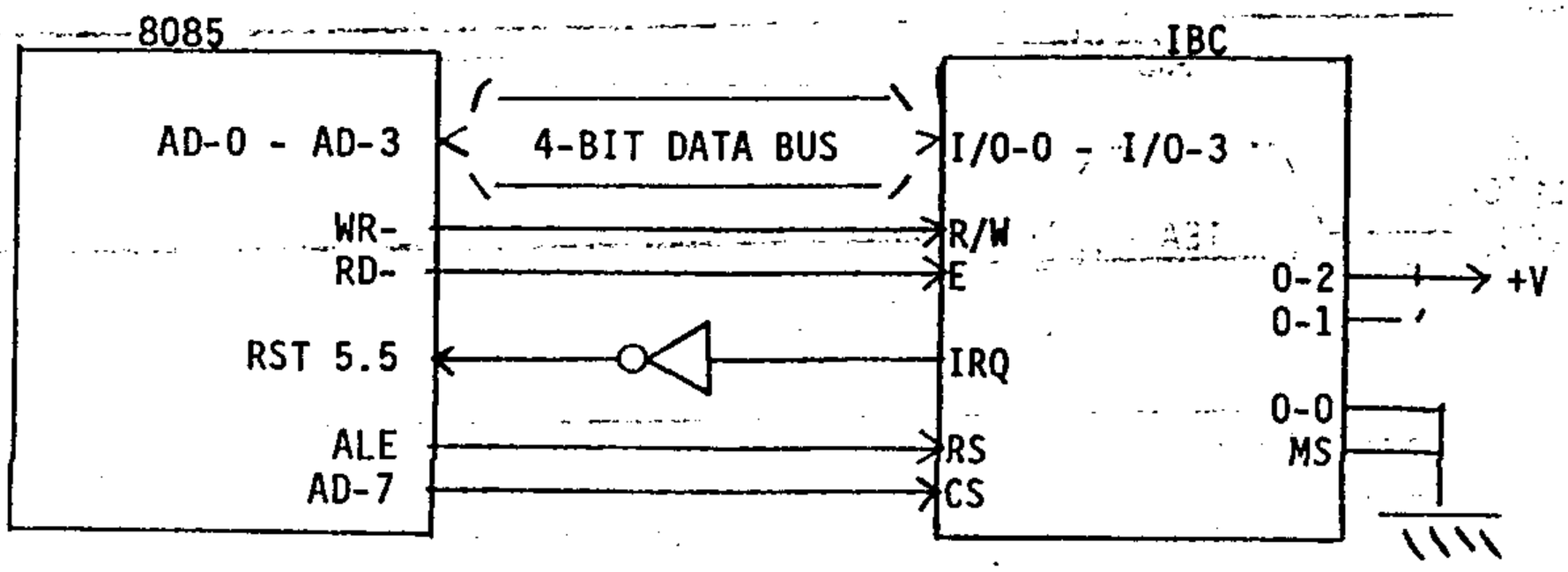
9.5 MODE 5 SPECIFICATIONS:

MODE 5 SPECIFICATIONS ARE THE SAME AS IN MODE 4 EXCEPT PULSE ON "ENABLE" LINE IS INVERTED.

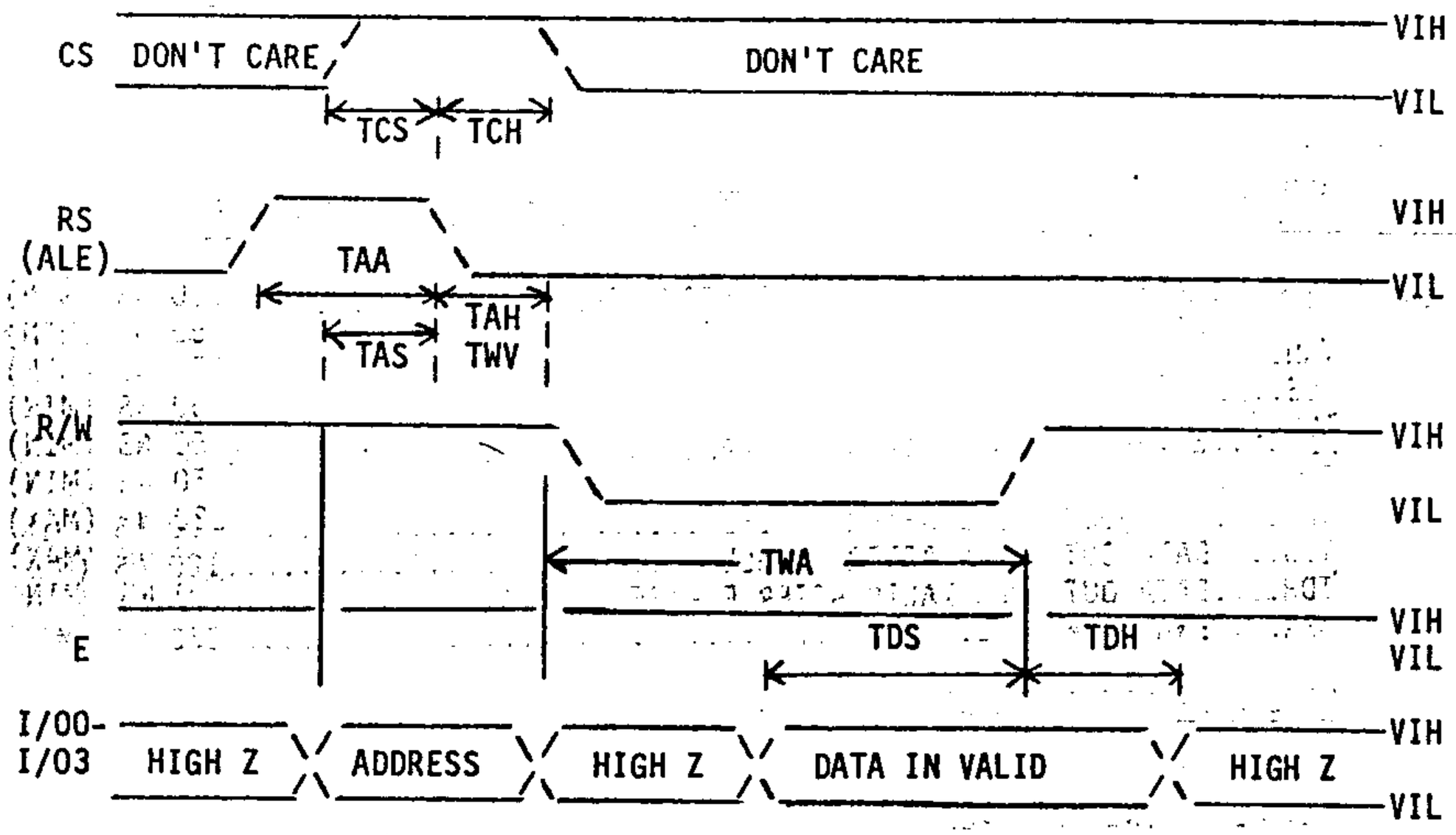
SIZE		DRAWING NO.
A		1052911
SCALE	REV A	SHEET 20

9.6 MODE 6 SPECIFICATIONS:

9.6.1 MODE 6 INTERFACE CONFIGURATION:

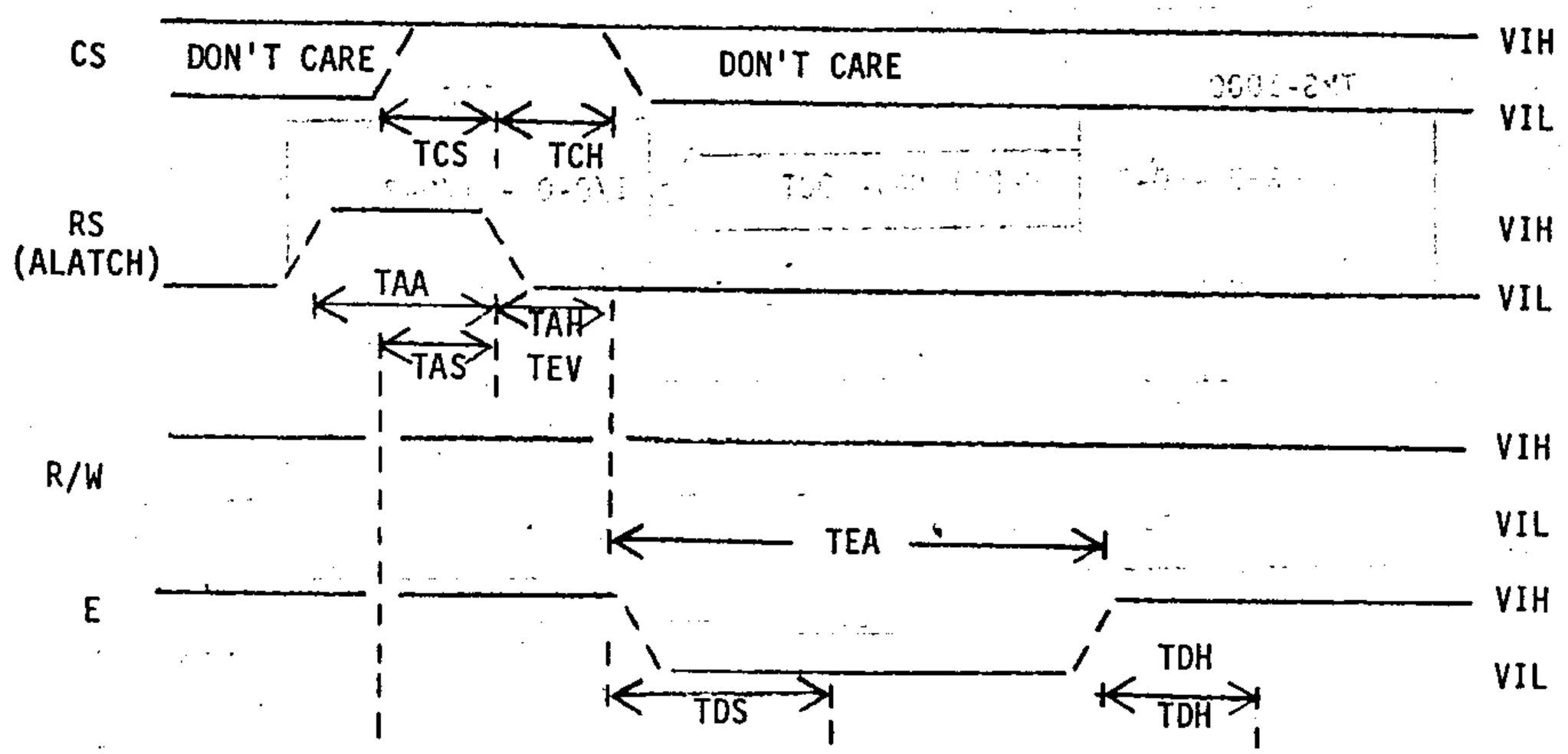


9.6.2 MODE 6 WRITE SEQUENCE AC CHARACTERISTICS:



TAA.....ALE PULSE WIDTH ON RS PIN..... 80 NS (MIN)
TAS.....ADDRESS VALID BEFORE RS(ALE) FALL..... 50 NS (MIN)
TAH.....ADDRESS HOLD VALID AFTER RS(ALE) FALL..... 50 NS (MIN)
TCS.....CHIP SELECT VALID BEFORE RS(ALE) FALL..... 50 NS (MIN)
TCH.....CHIP SELECT HOLD VALID AFTER RS(ALE) FALL..... 50 NS (MIN)
TWV.....R/W VALID AFTER RS(ALE) FALL..... 50 NS (MIN)
TDS.....DATA IN VALID BEFORE R/W RISE.....150 NS (MAX)
TDH.....DATA IN HOLD VALID AFTER R/W RISE..... 60 NS (MAX)
TWA.....WRITE PULSE WIDTH ON R/W PIN.....200 NS (MIN)

9.6.3 MODE 6 READ SEQUENCE AC CHARACTERISTICS:

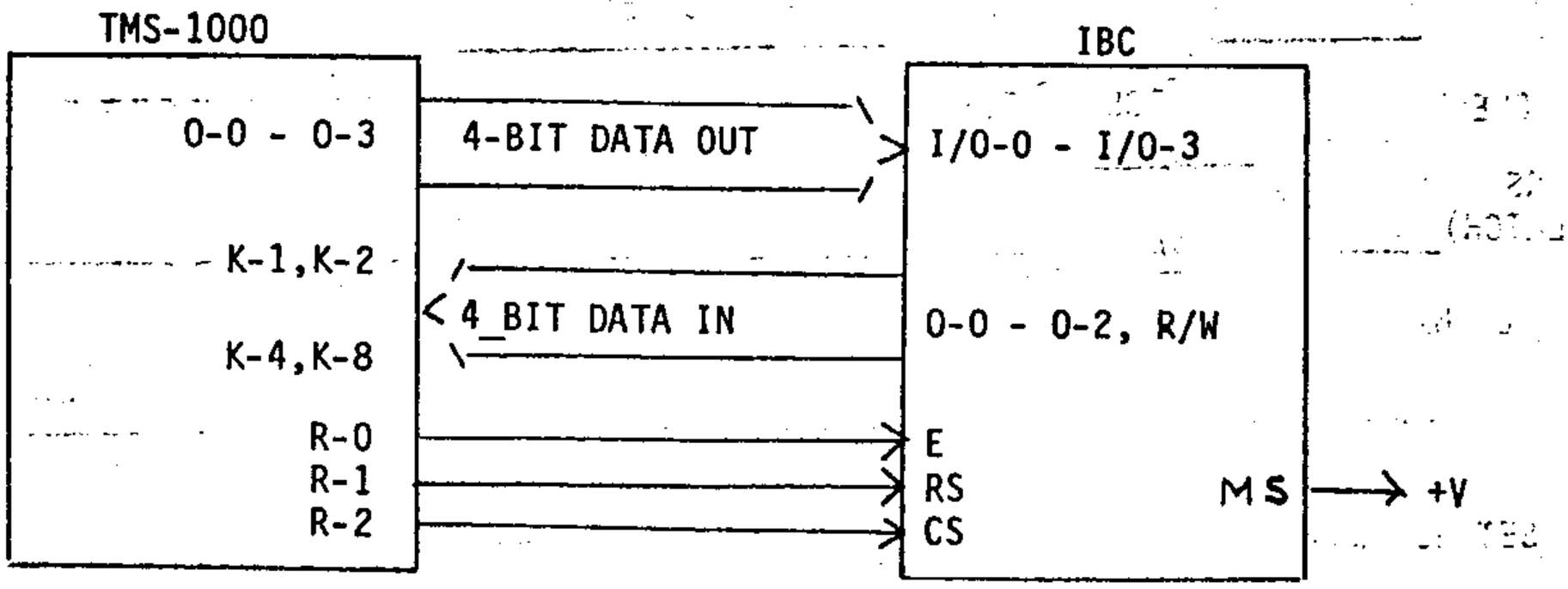


TAA.....ALE PULSE WIDTH ON RS PIN.....150 NS (MIN)
TAS.....ADDRESS VALID BEFORE RS(ALE) FALL..... 50 NS (MIN)
TAH.....ADDRESS HOLD VALID AFTER RS(ALE) FALL..... 50 NS (MIN)
TCS.....CHIP SELECT VALID BEFORE RS(ALE) FALL..... 50 NS (MIN)
TCH.....CHIP SELECT HOLD VALID AFTER RS(ALE) FALL..... 50 NS (MIN)
TEV.....E VALID AFTER RS(ALE) FALL..... 50 NS (MIN)
TDS.....DATA OUT VALID AFTER E FALL.....120 NS (MAX)
TDH.....DATA OUT HOLD VALID AFTER E RISE..... 60 NS (MAX)
TEA.....READ PULSE WIDTH ON E PIN.....200 NS (MIN)

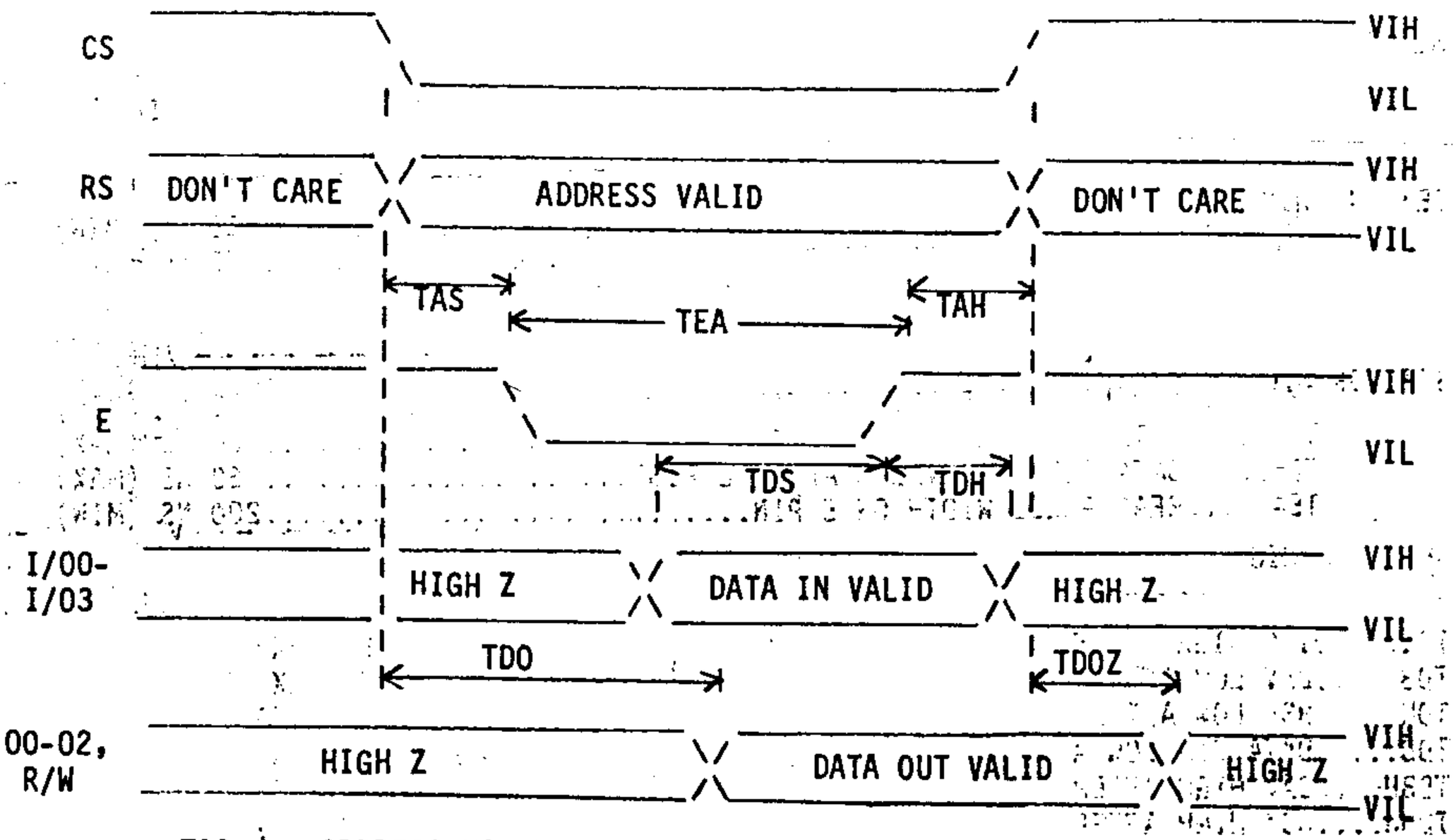
SIZE		DRAWING NO.
A		1052911
SCALE	REV A	SHEET 22

9.7 MODE 7 SPECIFICATION:

9.7.1 MODE 7 INTERFACE CONFIGURATION:

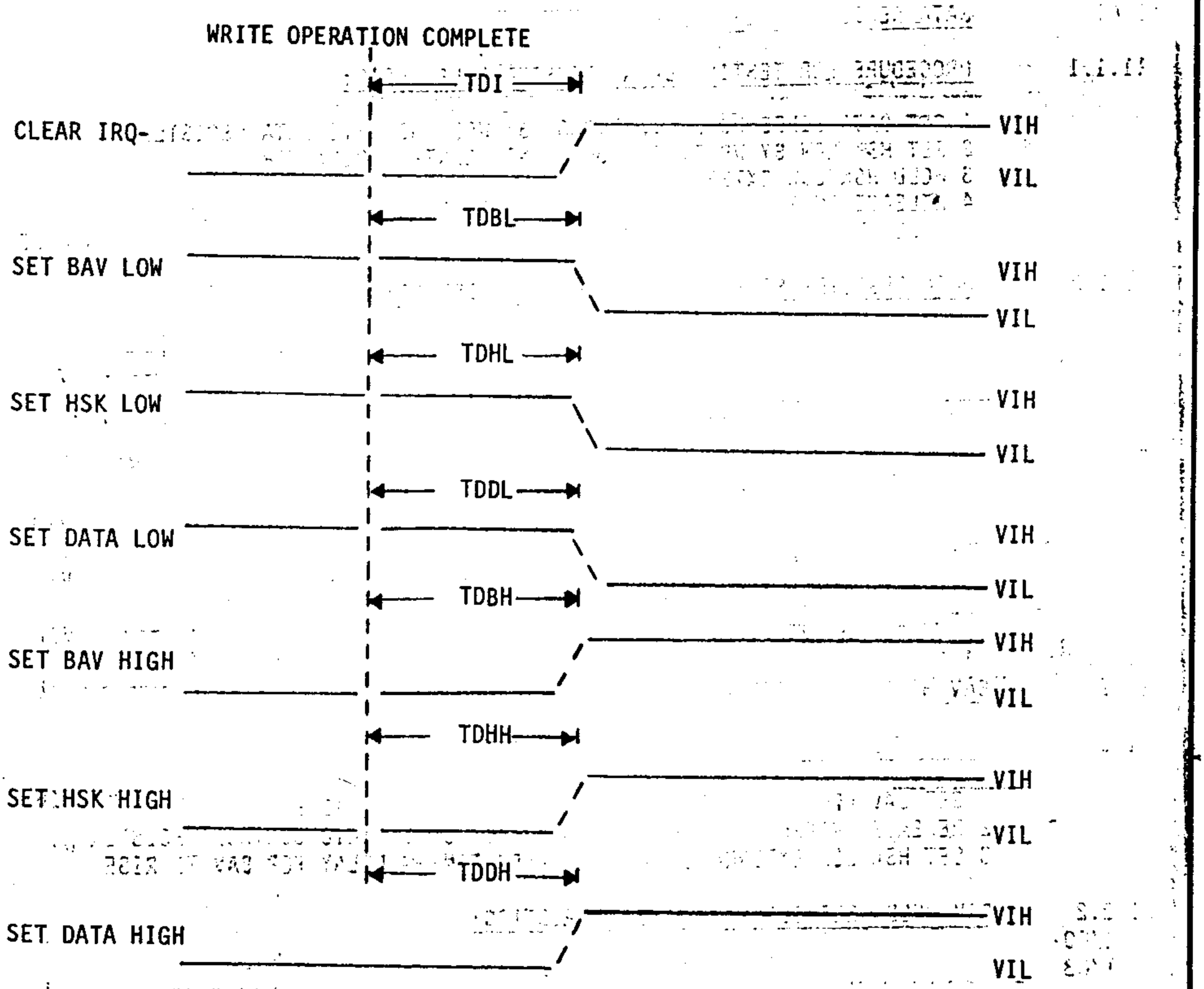


9.7.2 MODE 7 AC CHARACTERISTICS:



TAS.....ADDRESS VALID BEFORE E FALL..... 50 NS (MIN)
TAH.....ADDRESS HOLD VALID AFTER E RISE..... 50 NS (MIN)
TDS.....DATA IN VALID BEFORE E RISE.....120 NS (MAX)
TDH.....DATA IN HOLD VALID AFTER E RISE.....60 NS (MAX)
TDO.....DATA OUT VALID AFTER CS FALL..... 60 NS (MAX)
TDO.....DATA OUT VALID AFTER CS RISE.....60 NS (MAX)
TEA.....WRITE PULSE WIDTH ON E PIN.....200 NS (MIN)

10.0 PERIPHERAL BUS INTERFACE AC CHARACTERISTICS:



TDI.....IRQ HIGH AFTER WRITE CYCLE COMPLETION.....200 NS (MAX)
TDB.....BAV LOW AFTER WRITE CYCLE COMPLETION.....200 NS (MAX)
TDH.....HSK LOW AFTER WRITE CYCLE COMPLETION.....200 NS (MAX)
TDD.....DATA PIN LOW AFTER WRITE CYCLE COMPLETION.....200 NS (MAX)
TDBH....BAV HIGH AFTER WRITE CYCLE COMPLETION.....200 NS (MAX)
TDHH....HSK HIGH AFTER WRITE CYCLE COMPLETION.....200 NS (MAX)
TDDH....DATA PIN HIGH AFTER WRITE CYCLE COMPLETION.....200 NS (MAX)

TBD - BUS DELAY TIMING DEPENDS ON PULL-UP VALUE AND NUMBER OF PERIPHERALS ON THE BUS.

WRITE CYCLE COMPLETION MEANS END OF THE WRITE PULSE ON E OR R/W PINS CORRESPONDING TO THE MODE SELECTED AND ASSUMING THAT THE RIGHT COMMAND IS EXECUTED.

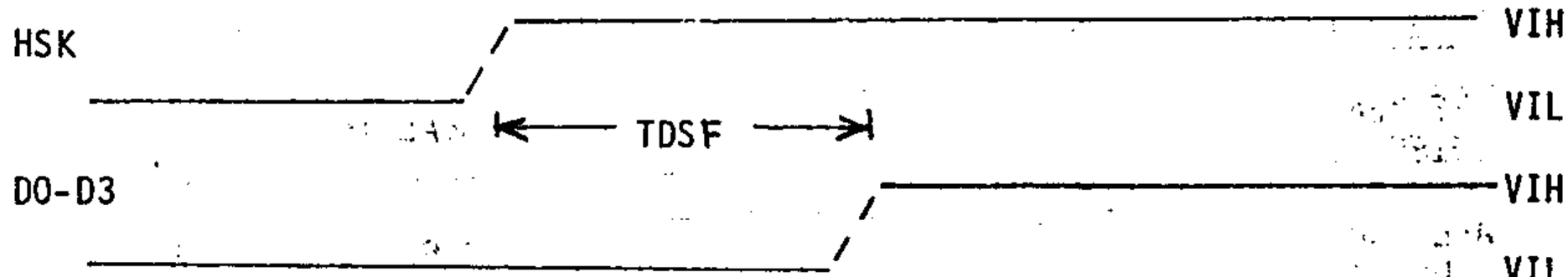
11.0 SPECIAL FUNCTIONS SPECIFICATIONS:

11.1 DATA REGISTER SELF-CLEAR:

11.1.1 PROCEDURE FOR TESTING DATA REGISTER SELF-CLEAR:

1 SET DATA LINES D0-D3 TO "0000" BY WRITING INTO DATA REGISTER
2 SET HSK LOW BY WRITING "0001" INTO CONTROL REGISTER
3 HOLD HSK LOW EXTERNALLY
4 RELEASE INTERNAL HSK BY WRITING "0000" INTO CONTROL REGISTER
5 RELEASE HSK EXTERNALLY AND OBSERVED TIME DELAY FOR DATA LINES TO RISE

11.1.2 DATA REGISTER SELF-CLEAR AC CHARACTERISTICS:



TDSF.....DATA LINES HIGH AFTER HSK RISE.....200 NS (MAX) + TBD

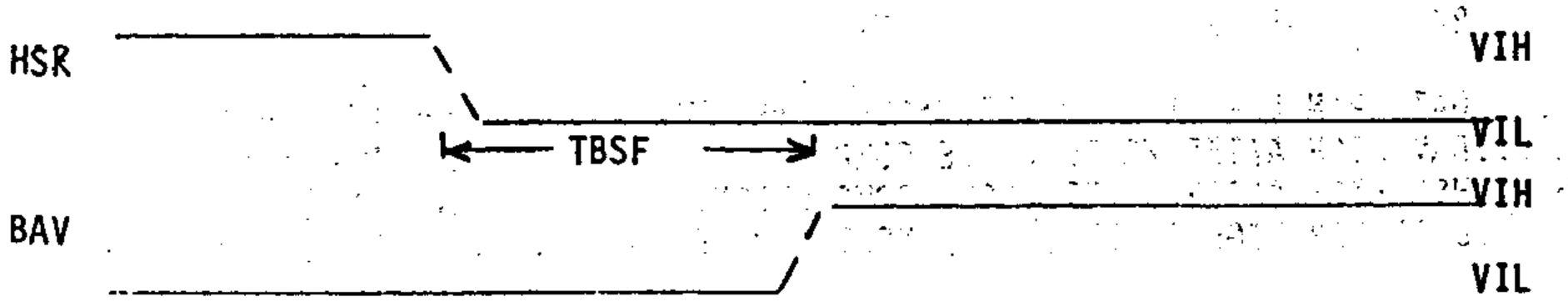
TBD - BUS DELAY TIMING DEPENDS ON PULL-UP VALUE AND NUMBER OF PERIPHERALS ON THE BUS.

11.2 BAV HOLD LATCH SELF-CLEAR:

11.2.1 PROCEDURE FOR TESTING BAV HOLD LATCH SELF-CLEAR:

1 SET BAV LOW BY WRITING "0010" INTO CONTROL REGISTER
2 RELEASE INTERNAL BAV HOLD BY WRITING "0000" INTO CONTROL REGISTER
3 SET HSK LOW EXTERNALLY AND OBSERVED TIMING DELAY FOR BAV TO RISE

11.2.2 BAV HOLD SELF-CLEAR AC CHARACTERISTICS:



TDSF.....INTERNAL BAV RELEASE AFTER HSK FALL.....200 NS (MAX) + TBD

TBD - BUS DELAY TIMING DEPENDS ON PULL-UP VALUE AND NUMBER OF PERIPHERALS ON THE BUS.

SECTION 4

ELECTRICAL CHARACTERISTICS

HEX BUS DC SPECIFICATION

OPERATING TEMPERATURE = 0C - 70 C

SYMBOL	CONDITIONS	MIN.	MAX	UNITS
Vdd (OF DEVICE ON BUS)	REF. VOLTAGE	4.5	5.5	V
Vil (RECOGNIZABLE)	ANY INPUT	0	0.8	V
Vih (RECOGNIZABLE)	ANY INPUT	4.0	5.5	V
Vol (ISINK= 8.0mA)	ANY OUTPUT		0.4	V
Voh	ANY OUTPUT	*	*	V
Iol (VOL = 0.4V)	ANY OUTPUT		8.0	mA
Iin/line	EACH DEVICE	-2	+2	uA
Rpullup/line	EACH DEVICE	8.2-10%	8.2+10%	K OHM
Cin/line (EXCLUDING CABLE CAPACITANCE	EACH DEVICE		30	pF
NUMBER OF EQUIVALENT DEVICES ON THE BUS			11	UNITS

* USE 8.2K OHM PULL-UPS TIED TO AN ALLOWABLE Vdd LEVEL.

12.0 QUALITY ASSURANCE PROVISIONS:

12.1 RESPONSIBILITY FOR INSPECTION:

UNLESS OTHERWISE SPECIFIED IN THE CONTRACT OR PURCHASE ORDER, THE SUPPLIER SHALL BE RESPONSIBLE FOR THE PERFORMING INSPECTIONS THAT ARE SUFFICIENT TO ASSURE THAT THE PARTS SUPPLIED MEET THE REQUIREMENTS SPECIFIED HEREIN.

12.2 LOT ACCEPTANCE:

LOTS FURNISHED TO THIS SPECIFICATION SHALL BE CAPABLE OF PASSING A SAMPLING INSPECTION FOR DEFECTS TO AN ACCEPTABLE QUALITY LEVEL (AQL) OF ONE PERCENT FOR NORMAL SINGLE SAMPLING, LEVEL II, PER MIL-STD-105. FAILING LOTS SHALL BE SUBJECTED TO REJECTION.

12.3 LIFE FAILURE RATE:

THE MEAN LIFE FAILURE RATE FOR DEVICES SHALL BE EQUAL TO OR LESS THAN .018%/1000 HOURS AT 55°C DERATED AT 0.5 EV.

12.3.1 ALL PARTS SHALL BE FUNCTIONALLY TESTED AFTER BEING BURNED IN FOR 24 HOURS AT 125°C AT NOMINAL DC VOLTAGES AND FOR A MINIMUM OF EIGHT HOURS AT 125°C AT RECOMMENDED HIGH STRESS VOLTAGES.

13.0 PREPARATION FOR DELIVERY:

13.1 PACKAGING:

PACKING AND WRAPPING SHALL BE SUFFICIENT TO PROTECT AGAINST DAMAGE OR LOSS DURING SHIPMENT FROM THE SUPPLIER TO THE DESTINATION SPECIFIED IN THE PURCHASE ORDER.

13.2 MARKING:

THE SHIPPING CONTAINER SHALL BE MARKED WITH TI PART NUMBER (SEE PART NUMBER BLOCK) AND THE QUANTITY CONTAINED. ADDITIONAL MARKINGS ARE PERMITTED.

14.0 SUGGESTED SOURCE(S) OF SUPPLY:

1. LSI LOGIC CORPORATION
1601 McCARTHY BOULEVARD
MILPITAS, CA 95035

TI PART NUMBER	MANUFACTURER'S PART NUMBER		
	SOURCE 1	SOURCE 2	SOURCE 3
1052911-1			

SIZE A		DRAWING NO. 1052911	
SCALE	REV A		SHEET 27

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